(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 945 844 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
29.09.1999 Bulletin 1999/39

(51) Int. Cl.[6]: G09G 3/28

(21) Application number: 98309013.5

(22) Date of filing: 04.11.1998

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 26.03.1998 JP 7966098

(71) Applicant: FUJITSU LIMITED
Kawasaki-shi, Kanagawa 211-8588 (JP)

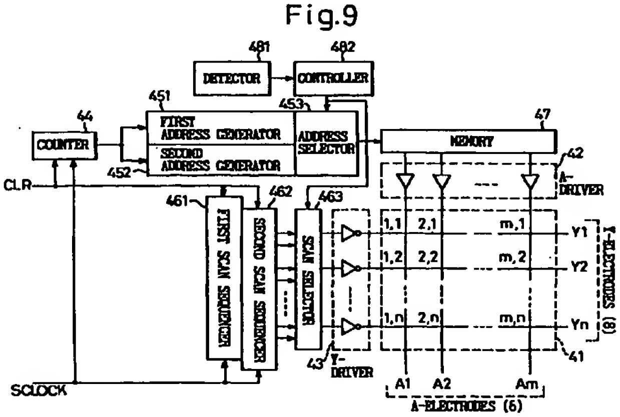
(72) Inventors:
- Tajima, Masaya
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- Okayasu, Junichi
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- Takata, Kiyoshi
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- Ishida, Katsuhiro
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- Fujisaki, Takashi
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- Awata, Yoshimasa
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- Kondo, Nobuyoshi
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- Tanaka, Shinsuke
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- Matsui, Naoki
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- Asami, Fumitaka
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)

(74) Representative:
Hitching, Peter Matthew et al
Haseltine Lake & Co.,
Imperial House,
15-19 Kingsway
London WC2B 6UD (GB)

(54) Display and method of driving the display

(57) A display has a panel (41), and first (6) and second (8) electrodes. The first and second electrodes define a matrix of cells on the panel. The second electrodes, which correspond to lines of the cells, are scanned to select the cell lines one by one. The first electrodes are driven to set display data for a selected one of the cell lines. The display also has a sequence setting unit (461, 462) for setting sequences of scanning the second electrodes, and a sequence selection unit (463) for selecting one of the sequences that minimizes the current and power consumption of a first-electrode driver (42) without deteriorating the quality of the displayed images.

Fig.9



EP 0 945 844 A2

Printed by Xerox (UK) Business Services
2.16.7/3.6

Description

[0001] The present invention relates to displays and a method of driving a display, and more particularly to displays having a matrix of electrodes that is scanned line by line to set display data, such as plasma display panels (PDPs), electroluminescence (EL) panels, and liquid-crystal displays (LCDs), and a method of driving such displays.

[0002] Displays such as PDPs, EL panels, and liquid-crystal displays are getting larger in size and capacity and acquiring full-color display capabilities. As a result, the power consumption of the displays is increasing. It is necessary to minimize the power consumption of the displays.

[0003] For example, in a three-electrode surface-discharge alternating-current plasma display panel (3-electrode, surface-discharge AC PDP), a frame is divided into a plurality of sub-frames, in order to display gradations on the PDP. These sub-frames have respective sustain periods whose lengths differ from one another to display gradation levels in combination, and each sub-frame consists of a reset period, an addressing period, and a sustain period. The reset period sets all of the Y-electrodes and applies write pulses to all of the addressing electrodes and X-electrodes. As a result, every cell causes a discharge and neutralizes itself (self-erase discharge).

[0004] In previously proposed PDPs, the Y-electrodes have only been sequentially scanned and this sequence has never been changed. Further, the resolution of displays, i.e. the number of lines on the screen of a display, has been increased, which has led to an increase in the electrode-to-electrode capacitance.

charging & discharge

[0005] The power consumption associated with charging and discharging the electrodes constitutes a large part of the power consumption of the PDP. Therefore, the power required to charge and discharge the electrodes must be reduced to reduce the overall power consumption.

frequency

[0006] The power required to charge and discharge electrodes is determined by the capacitance, driving voltage, and driving frequency of the electrodes. Among them, only the driving frequency is controllable. A conventional technique drops the driving frequency by masking display data or by reducing the number of sub-frames in each frame. This technique results in reducing the number of gradation levels to be displayed, thereby deteriorating the quality of images to be displayed.

[0007] It is desirable to provide a display capable of reducing its current and power consumption without deteriorating the quality of displayed images, and a method of driving such a display.

[0008] According to an embodiment of a first aspect of the present invention, there is provided a display having a panel, and first and second electrodes; the first and second electrodes defining a matrix of cells on the panel; the second electrodes, which correspond to lines of the cells, being scanned to select cell lines one by one; the first electrodes being driven to set display data for a selected one of the cell lines, wherein the display comprises a sequence setting unit for setting sequences of scanning the second electrodes; and a sequence selection unit for selecting one of the sequences.

[0009] The display may further comprise a difference detection unit for detecting differences between display data set for the cell lines so that one of the sequences that minimizes the differences is selected. The display may further comprise a difference detection unit for detecting differences between display data set for the cell lines; and an upper limit setting unit for setting an upper limit so that one of the sequences that suppresses the differences to below the upper limit is selected. The sequences may be set based on powers of two. The sequence setting unit may divide the second electrodes into blocks and sets sequences of scanning the second electrodes block by block, and the sequence selection unit may select one of the sequences in each of the blocks.

[0010] The first electrodes may be addressing electrodes, and the second electrodes may be scan electrodes. The display may further comprise an address driver for driving the addressing electrodes; a current/power value detection unit for detecting a current or power value of the address driver; and a sequence changing unit for changing a sequence of scanning the second electrodes to minimize the current or power value.

[0011] The display may further comprise a current/power value evaluation unit for evaluating a current or power value of the address driver according to display data set for the cell lines so that one of the sequences that minimizes the current or power value is selected. The display may further comprise a reference value setting unit for setting a reference value so that one of the sequences that suppresses the current or power value to below the reference value is selected.

L

[0012] The display may further comprise a current/power value evaluation unit for evaluating a current or power value of the address driver according to display data set for the cell lines; and a reference value setting unit for setting a reference value so that one of the sequences that suppresses the current or power value to below the reference value is selected. The display may further comprise a current/power value evaluation unit for evaluating a current or power value of the address driver beforehand according to display data set for the cell lines; and a reference value setting unit for setting a reference value so that one of the sequences that suppresses the current or power value to below the reference value is selected. The display may further comprise a display data supplying unit for supplying display data line by line to the first electrodes according to the selected sequence of scanning the second electrodes.

[0013] The display may be a plasma display; a frame of display data may be divided into a plurality of sub-frames that are selectively combined to display gradations; and each of the sub-frames may at least include an addressing period and a sustain period. The panel may be a three-electrode surface-discharge alternating-current plasma display panel having third electrodes that run in parallel with the second electrodes and applying an alternating voltage to the second and third electrodes to repeat a sustain discharge.

[0014] Further, according to an embodiment of a second aspect of the present invention, there is provided a display having a panel, and first and second electrodes; the first and second electrodes defining a matrix of cells on the panel; the second electrodes, which correspond to lines of the cells, being scanned to select cell lines one by one; the first electrodes being driven to set display data for a selected one of the cell lines, wherein the display comprises a sequence setting unit for optionally setting a sequence of scanning the second electrodes.

[0015] The display may further comprise a difference detection unit for detecting differences between display data set for the cell lines so that the second electrodes are scanned in a sequence to minimize the differences. The display may further comprise a difference detection unit for detecting differences between display data set for the cell lines; and an upper limit setting unit for setting an upper limit so that the second electrodes are scanned in a sequence to suppress the differences to below the upper limit. The sequence setting unit may divide the second electrodes into blocks and sets a sequence of scanning the second electrodes in each of the blocks.

[0016] The first electrodes may be addressing electrodes, and the second electrodes may be scan electrodes. The display may further comprise an address driver for driving the addressing electrodes; a current/power detection unit for detecting a current or power value of the address driver; and a sequence changing unit for changing a sequence of scanning the second electrodes to minimize the current or power value.

[0017] The display may further comprise a current/power evaluation unit for evaluating a current or power value of the address driver according to display data set for the cell lines so that the second electrodes are scanned in a sequence to minimize the current or power value. The display may further comprise a reference value setting unit for setting a reference value so that the second electrodes are scanned in a sequence to suppress the current or power value to below the reference value. The display may further comprise a current/power evaluation unit for evaluating a current or power value of the address driver according to display data set for the cell lines; and a reference value setting unit for setting a reference value so that the second electrodes are scanned in a sequence to suppress the current or power value to below the reference value. The display may further comprise a current/power evaluation unit for evaluating a current or power value of the address driver beforehand according to display data set for the cell lines; and a reference value setting unit for setting a reference value so that the second electrodes are scanned in a sequence to suppress the current or power value to below the reference value.

[0018] The display may further comprise a display data supplying unit for supplying display data line by line to the first electrodes according to the determined sequence of scanning the second electrodes. The display may be a plasma display; a frame of display data may be divided into a plurality of sub-frames that are selectively combined to display gradations; and each of the sub-frames may at least include an addressing period and a sustain period. The panel may be a three-electrode surface-discharge alternating-current plasma display panel having third electrodes that run in parallel with the second electrodes and applying an alternating voltage to the second and third electrodes to repeat a sustain discharge.

[0019] According to an embodiment of a third aspect of the present invention, there is provided a method of driving a display having a panel, and addressing and scan electrodes, the addressing and scan electrodes defining a matrix of cells on the panel; the scan electrodes, which correspond to lines of the cells, being scanned to select the cell lines one by one; the addressing electrodes being driven to set display data for a selected one of the cell lines, wherein the method comprises the steps of setting sequences of scanning the scan electrodes; detecting a current or power value of an address driver for driving the addressing electrodes; and selecting one of the sequences in accordance with the detected current or power value.

[0020] The sequences may be set based on powers of two.

[0021] Further, according to an embodiment of a fourth aspect of the present invention, there is provided a method of driving a display having a panel, and addressing and scan electrodes, the addressing and scan electrodes defining a matrix of cells on the panel; the scan electrodes, which correspond to lines of the cells, being scanned to select the cell lines one by one; the addressing electrodes being driven to set display data for a selected one of the cell lines, wherein the method comprises the steps of detecting a current or power value of an address driver for driving the addressing electrodes; and optionally setting a sequence of scanning the scan electrodes in accordance with the detected current or power value.

[0022] The method may further comprise the steps of dividing the scan electrodes into blocks; and setting a sequence of scanning the scan electrodes in each of the blocks.

[0023] Reference will now be made, by way of example, to the accompanying drawings, in which:

Fig. 1 shows a previously-considered 3-electrode, surface-discharge AC PDP;

Fig. 2 is a sectional view taken along an addressing electrode showing the structure of a cell of the PDP of Fig. 1;

Fig. 3 is a sectional view taken along a sustain electrode showing the structure of the cell of Fig. 2;

Fig. 4 is a block diagram showing a display employing the PDP of Fig. 1;

Fig. 5 is a timing chart showing a gradation control technique using sub-frames carried out on the PDP display of Fig. 4;

Fig. 6 shows waveforms for driving the PDP display of Fig. 4;

Fig. 7 is a block diagram showing a previously-considered display;

Fig. 8 is a timing chart showing the operation of the display of Fig. 7;

Fig. 9 is a block diagram showing a display according to a first embodiment of the present invention;

Fig. 10 is a timing chart showing the operation of the display of Fig. 9;

Fig. 11 is a flowchart showing a control sequence of the display of Fig. 9;

Figs. 12A to 12C show changes occurring in electrodes when displaying a pattern;

Figs. 13A to 13C show changes occurring in electrodes when displaying another pattern;

Figs. 14 to 16 show changes occurring in electrodes with respect to different patterns;

Fig. 17 is a block diagram showing a display according to a second embodiment of the present invention;

Fig. 18 is a timing chart showing a 3-line-jump operation of the display of Fig. 17;

Fig. 19 shows the operation of a sequential address generator of the display of Fig. 17;

Fig. 20 shows the operation of a 1-line-jump address generator of the display of Fig. 17;

Fig. 21 shows the operation of a 3-line-jump address generator of the display of Fig. 17;

Fig. 22 is a block diagram showing a display according to a third embodiment of the present invention;

Fig. 23 is a block diagram showing a display according to a fourth embodiment of the present invention;

Fig. 24 is a block diagram showing a difference detector circuit of the display of Fig. 23;

Fig. 25 is a block diagram showing a difference detector contained in the difference detector circuit of Fig. 24;

Fig. 26 shows a circuit for generating control signals for latches contained in the difference detector circuit of Fig. 24;

Fig. 27 is a timing chart showing the operation of the difference detector circuit of Fig. 24;

Fig. 28 is a block diagram showing a scan sequencer of the display of Fig. 23; and

Fig. 29 shows the operation of an address generator of the display of Fig. 23.

[0024] For a better understanding of the preferred embodiments of the present invention, some of the problems associated with previously-considered displays will first be explained.

[0025] There are known flat displays that employ PDPs (plasma display panels), EL (electroluminescence) elements, LCDs (liquid-crystal displays), VFDs (vacuum fluorescent displays), and LEDs (light emitting diodes). Embodiments of the present invention are applicable to any of these displays. Hereafter, embodiments of the present invention are explained in connection with plasma displays, in particular, three-electrode surface-discharge alternating-current plasma displays (3-electrode, surface-discharge AC plasma displays).

[0026] An AC plasma display has two types of sustain electrodes, i.e. X- and Y-electrodes to which pulses are alternately applied to repeatedly discharge the electrodes and emit light therefrom. One period of discharge lasts for one to several microseconds after the application of a pulse. The discharge produces positively charged ions and negatively charged electrons. The ions accumulate on an insulation layer over an electrode to which a negative voltage is applied, and the electrons accumulate on the insulation layer over an electrode to which a positive voltage is applied. These accumulated ions and electrons are generally called "wall charge."

[0027] To make a target cell of the display emit light, a write pulse of high voltage is applied thereto. The write pulse causes a discharge to accumulate wall charge in the cell. A sustain pulse whose polarity is opposite to that of the write pulse and whose voltage is lower than that of the write pulse is applied to the cell. The sustain pulse causes a discharge to increase the wall charge. This increases a voltage with respect to a discharge space in the cell above a discharge threshold, to start a discharge in the cell. Once a cell of the display accumulates wall charge due to a write discharge, the cell repeats a discharge whenever sustain pulses of opposite polarities are alternately applied thereto. This is called a memory effect or a memory function of the cell. AC PDPs use the memory effect to display information thereon.

[0028] There are 2-electrode AC PDPs and 3-electrode AC PDPs. The 2-electrode AC PDPs employ two electrodes to carry out addressing discharge and sustain discharge in each cell. The 3-electrode AC PDPs additionally employ electrodes of a third type to carry out addressing discharge in each cell. Color PDPs for displaying gradations cause discharge in cells to produce ultraviolet rays that excite phosphor contained in the cells. The phosphor is vulnerable to the impact of positively charged ions that are produced when the cells are discharged. The 2-electrode AC PDPs have a struc-

ture to make ions directly hit the phosphor, which shortens the service life of the phosphor.

[0029] To avoid this, the 3-electrode AC PDPs are usually used for color displays. There are two types of 3-electrode AC PDPs. One type arranges two types of sustain electrodes, i.e. X- and Y-electrodes as well as electrodes of a third type on the same substrate. The other type arranges X- and Y-electrodes on a substrate and third electrodes on an opposite substrate. The PDPs that form the three types of electrodes on the same substrate are classified into two categories. One category forms the third electrodes on the sustain electrodes, and the other forms the third electrodes under the sustain electrodes. There are transmission PDPs that make phosphors emit and transmit visible light toward viewers, and there are reflection PDPs that make phosphors emit and reflect visible light toward viewers. Cells of the PDPs are spatially isolated from one another by barriers. Some PDPs surround every cell with barriers so that the cells are completely isolated from one another. Some PDPs form barriers along opposite edges of each cell and isolate the other opposite edges by proper electrode gaps.

[0030] Each example mentioned below relates to a reflection-type PDP display having two types of sustain electrodes on a substrate, addressing electrodes on an opposite substrate, and barriers along the addressing electrodes orthogonally to the sustain electrodes. Each sustain electrode is partly formed with a transparent electrode. Embodiments of the present invention are also applicable to other types of PDP displays, EL displays, LCDs, VFDs, LED displays, etc.

[0031] Previously-proposed displays will now be explained in more detail. Figure 1 shows a previously-considered 3-electrode, surface-discharge AC PDP. Figure 2 is a sectional view taken along an addressing electrode showing one light emitting cell of the PDP of Fig. 1. Figure 3 is a sectional view taken along a line L0 of Fig. 2, showing the cell of Fig. 2.

[0032] The PDP 1 includes barriers 2, the cells 3 for emitting light, a front substrate 4 made of glass, a rear substrate 5 made of glass, addressing electrodes 6, X-electrodes 7, Y-electrodes 8, phosphor 9, a dielectric layer 10, and a protective film 11 made of MgO.

[0033] The PDP 1 is basically structured with the substrates 4 and 5. The X-electrodes 7 and Y-electrodes 8 (Y1 to Yn) run in parallel with one another and are formed on the front substrate 4. The front substrate 4 faces the rear substrate 5 on which the addressing electrodes 6 (A1 to Am) are formed orthogonally to the X- and Y-electrodes. Each of the X-electrodes 7 is made of a transparent electrode 71 and a bus electrode 72. Each of the Y-electrodes 8 is made of a transparent electrode 81 and a bus electrode 82. The X- and Y-electrodes serve as sustain electrodes to which an AC voltage is applied to trigger sustain discharge.

[0034] The phosphor 9 produces a reflected beam 12. To transmit the reflected beam 12, the transparent electrodes 71 and 81 are made of, for example, ITO whose main component is an indium oxide that is transparent. The bus electrodes 72 and 82 are made of low-resistance metal such as Cr (chrome) and Cu (copper) to prevent a voltage drop due to electrode resistance. The transparent electrodes 71 and 81 and bus electrodes 72 and 82 are covered with the dielectric layer 10 made of, for example, glass to insulate the electrodes. The dielectric layer 10 is covered with the protective film 11 made of MgO (magnesium oxide).

[0035] The addressing electrodes 6 are formed on the rear substrate 5 that faces the front substrate 4. The addressing electrodes 6 are orthogonal to the sustain electrodes 7 and 8. The barrier 2 is formed between the adjacent addressing electrodes 6. The addressing electrode 6 between the adjacent barriers 2 is covered with the phosphor 9 having a light emitting characteristic of red, green, or blue.

[0036] The ridges of the barriers 2 are attached to the protective film 11, and a discharge gas is sealed between the substrates 4 and 5, to complete the cells 3 of the PDP 1. The cells 3 are bordered with the barriers 2 and are positioned at intersections of the sustain electrodes 7 and 8 and the addressing electrodes 6. Discharge in the cell 3 is mainly caused by the sustain electrodes 7 and 8. A given cell is selected by a discharge caused by the corresponding addressing electrode 6 and Y-electrode 8.

[0037] A discharge space in each cell is separated by the barriers 2 so that the cell may discretely cause discharge. The discharge produces ultraviolet rays, which make the phosphor 9 emit a beam to produce the reflection beam 12. The cells 3 are arranged in an "m x n" matrix to form the PDP 1. The addressing electrodes 6 range from A1 to Am, and Y-electrodes 8 from Y1 to Yn. The X-electrodes 7 are commonly connected together.

[0038] Figure 4 is a block diagram showing a PDP display employing the PDP 1 of Fig. 1. The PDP display has peripheral circuits for driving the PDP 1.

[0039] The display includes a control circuit 27, a display data controller 28, a frame memory 29, a panel controller 20, a scan driver controller 21, a common driver controller 22, an address driver 23, a Y-driver 24, a common Y-driver 25, and a common X-driver 26.

[0040] The display employs a dot clock signal CLOCK, display data DATA (for example, 8-bit display data for each of three primary colors to realize 256 gradations), a vertical synchronizing signal VSYNC to indicate the start of a frame, and a horizontal synchronizing signal HSYNC to indicate the start of a line.

[0041] The control circuit 27 has the display data controller 28 and panel controller 20. The display data controller 28 stores display data in the frame memory 29 and provides the address driver 23 with the display data and control signals including a transfer clock signal according to the driving timing of the PDP 1. The panel controller 20 determines the timing of a high-voltage waveform applied to the PDP 1 and has the scan driver

controller 21 and common driver controller 22.

[0042] The addressing electrodes A1 to Am are individually connected to the address driver 23, which applies addressing pulses to the addressing electrodes to cause addressing discharge. The Y-electrodes Y1 to Yn are individually connected to the Y-driver 24, which is connected to the common Y-driver 25. The Y-driver 24 generates pulses to select a line during an addressing period. The common Y-driver 25 generates sustain pulses, which are applied to the Y-electrodes Y1 to Yn through the Y-driver 24. The X-electrodes 7 are commonly connected to cover all display lines of the PDP 1 and are controlled by the common X-driver 26 that is connected to the common driver controller 22. The common X-driver 26 generates write pulses and sustain pulses. These drivers are controlled by the control circuit 27, which is controlled by external signals including VSYNC, HSYNC, CLOCK, and DATA.

[0043] Figure 5 is a timing chart showing a gradation control technique using sub-frames carried out on the PDP display of Fig. 4, and Fig. 6 shows waveforms for driving the PDP display of Fig. 4.

[0044] To display gradations on the PDP display of Fig. 4, the technique of Fig. 5 divides a frame Tf into sub-frames 1SF to jSF (for example, j = 8) to which display data bits are assigned, respectively. The sub-frames 1SF to 8SF have respective sustain periods whose lengths differ from one another to display gradation levels in combination. If each piece of display data consists of "j" bits to realize 2^j gradation levels, every frame is divided into j sub-frames having sustain periods Ts-sf(j) of the ratio of 1:2:4:8:...:2^{j-1}. The sub-frames have each an identical addressing period Ta-sf.

[0045] Each sub-frame consists of a reset period, an addressing period, and a sustain period. The reset period sets all of the Y-electrodes Y1 to Yn to 0 V and applies write pulses to all of the addressing electrodes A1 to Am and X-electrodes 7. As a result, every cell causes a discharge and neutralizes itself. This is a self-erase discharge.

on - off
charge/discharge

[0046] [redacted]

[0047] In the addressing period, the address driver 23 applies addressing pulses A(1) to A(m) according to display data to the addressing electrodes A1 to Am. At the same time, the Y-driver 24 applies selection pulses to the Y-electrodes Y1 to Yn. During the sustain period, the common Y-driver 25 applies sustain pulses to the Y-electrodes Y1 to Yn. The X-electrodes 7 are commonly connected to the common X-driver 26, which applies common pulses to the X-electrodes.

[0048] [redacted]

[0049] Figure 7 is a block diagram showing a previously-considered display, and Fig 8 is a timing chart showing the operation of the display of Fig. 7.

[0050] The display has a panel 31, an address driver (A-driver) 32, a Y-driver 33, a line counter 34, an address generator 35, a shift register 36, and a memory 37. The A-driver 32, Y-driver 33, and memory 37 correspond to the address driver 23, Y-driver 24, and frame memory 29 of Fig. 4. The shift register 36 is installed in the scan driver controller 21, and the counter 34 and address generator 35 are installed in the display data controller 28 of Fig. 4. The memory 37 may consist of two frame memories so that data is written into one of them while data is transferred from the other to the panel 31 with the use of the sub-frame technique. In Fig 7, a frame of display data is present in the memory 37 and is read therefrom into the panel 31.

[0051] The shift register 36 is used to scan the panel 31 line by line according to shift data and a shift clock signal. The address generator 35 converts the output of the counter 34 into an address of the memory 37 at which display data for a presently scanned line of the panel 31 is read.

[0052] The operation of the display of Fig. 7 will be explained with reference to Fig. 8. To write data into the panel 31, the prior art applies a clear pulse CLR at the start of each of the sub-frames 1SF to jSF (Fig. 5). The Y-driver 33 sequentially selects the Y-electrodes Y1 to Yn in response to a scan clock signal SCLOCK. Display data for a scanned Y-electrode is supplied from the memory 37 to the A-driver 32, which applies the display data to the addressing electrodes A1 to Am.

[0053] More precisely, the counter 34 receives the clear pulse CLR and scan clock signal SCLOCK and makes the address generator 35 specify display data for a scanned Y-electrode. For example, if the Y-electrode Y1 is scanned, data pieces for cells (1, 1), (2, 1), (3, 1), ..., and (m, 1) on the Y-electrode Y1 are applied to the addressing electrodes A1 to Am. If the Y-electrode Y2 is scanned, data pieces for cells (1, 2), (2, 2), (3, 2), ..., and (m, 2) on the Y-electrode Y2 are applied to the addressing electrodes A1 to Am. If the Y-electrode Yn is scanned, data pieces for cells (1, n), (2, n), (3, n), ..., and (m, n) on the Y-electrode Yn are applied to the addressing electrodes A1 to Am.

[0054] In this way, the prior art scans the Y-electrodes only in a sequence of Y1, Y2, Y3, ..., Yn, and this sequence is never changed.

[0055] [redacted] presently scanned line. At this time, the power con- [redacted]

[0056] [redacted]

tance. The power consumption to charge and discharge the electrodes is a large part of the [redacted]

[0057] [redacted] electrodes is determined by the capacitance, driving voltage, and driving frequency of the electrodes. Among them, only the driving frequency is controllable. A conventional technique drops the driving frequency by masking display data or by reducing the number of sub-frames in each frame. This technique results in reducing the number of gradation levels to be displayed, thereby deteriorating the quality of images to be displayed.

[0058] Next, displays and display driving methods according to preferred embodiments of the present invention will be explained with reference to the drawings.

[0059] Figure 9 is a block diagram showing a display according to the first embodiment of the present invention, and Fig. 10 is a timing chart showing the operation of the display.

[0060] The display has a panel 41, an address driver (A-driver) 42, a Y-driver 43, a counter 44, a first address generator 451, a second address generator 452, an address selector 453, a first scan sequencer 461, a second scan sequencer 462, a scan selector 463, a memory 47, a detector 481, and a controller 482.

[0061] The A-driver 42, Y-driver 43, and memory 47 correspond to the address driver 23, Y-driver 24, and frame memory 29 of Fig. 4. The first scan sequencer 461, second scan sequencer 462, and scan selector 463 are installed in the scan driver controller 21 of Fig. 4. The counter 44, first address generator 451, second address generator 452, address selector 453, detector 481, and controller 482 are installed in the display data controller 28 of Fig. 4. Although the display of Fig. 9 has two address generators and two scan sequencers, the numbers of these devices are optional.

[0062] The first address generator 451 generates addresses of the memory 47 according to a Y-electrode scan sequence provided by the first scan sequencer 461. The second address generator 452 generates addresses of the memory 47 according to a Y-electrode scan sequence provided by the second scan sequencer 462. [redacted]

[0063] [redacted] A smaller one of the outputs [redacted] The output [redacted] If the detector 481 [redacted] of [redacted], and at the same time, [redacted]461.

[0064] The relationship between data read out of the memory 47 according to selection made by the address selector 453 and the Y-electrodes scanned according to selection made by the scan selector 463 is the same as that of the previously-considered displays, except the order of scanning the Y-electrodes.

[0065] An example of a data write operation to the panel 41 according to the first embodiment will be explained with reference to Fig. 10. At the start of each sub-frame (Fig. 5), a clear pulse CLR is applied. The Y-driver 43 scans the Y-electrodes Y1 to Yn according the output of the scan sequencer selected by the scan selector 463. At the same time, the address selector 453 selects the address generator that corresponds to the selected scan sequencer and supplies the output of the selected address generator to the memory 47. As a result, the A-driver 42 supplies display data corresponding to the scanned Y-electrode to the addressing electrodes A1 to Am.

[0066] For example, if the Y-electrodes are scanned in order of Y1, Y3, ..., and Yn-1, and then, Y2, Y4, ..., and Yn, display data is supplied to the addressing electrodes A1 to Am in order of (1, 1) to (m, 1), (1, 3) to (m, 3), ..., and (1, n-1) to (m, n-1), and then, (1, 2) to (m, 2), (1, 4) to (m, 4), ..., and (1, n) to (m, n).

[0067] [redacted] 41, [redacted]

[0068] Figure 11 is a flowchart showing a control sequence of the display of Fig. 9.

[0069] Step ST1 selects a scan sequence 1 to select the output of the first address generator 451. Step ST2 detects the power consumption "P1" of the A-driver 42, i.e. a current flowing to the A-driver 42 based on the scan sequence 1.

[0070] Step ST3 selects a scan sequence 2 to select the output of the second address generator 452. Step ST4 detects the power consumption "P2" of the A-driver 42 based on the scan sequence 2.

[0071] Step ST5 checks to see if P1 < P2. If P1 < P2, step ST7 selects the scan sequence 1 of smaller power consumption. Step ST8 detects a new power consumption value P1 based on the scan sequence 1. Step ST9 checks to see if P1 < P2. If P1 < P2, the flow returns to step ST8, and if not, the scan sequence 1 is maintained until P1 >= P2.

[0072] If P1 >= P2 in step ST5, step ST6 detects a new power consumption value P2 based on the scan sequence 2, and step ST5 is repeated. This loop is repeated to maintain the scan sequence 2 until step

ST5 determines that P1 < P2.

[0073] In this way, the first embodiment detects power consumption values P1 and P2 of the A-driver 42 based on scan sequences 1 and 2, compares the values P1 and P2 with each other, and always selects one of the scan sequences 1 and 2 that provides a lower power consumption value. Although the number of scan sequences is two in the above example, any number of scan sequences are employable for other embodiments of the present invention.

[0074] Figures 12A to 16 explain changes in electrodes with respect to various patterns to be displayed.

[0075] In Fig. 12A, a "4 x 4" matrix of 16 cells (pixels) displays a checkered pattern with Y-electrodes Y1 to Y4 and addressing electrodes (A-electrodes) A1 to A4.

[0076] Figure 12B shows a scan sequence that scans the Y-electrodes in order of Y1, Y2, Y3, and Y4. In this sequence, the levels of the A-electrodes A1 to A4 change from 0 to 1 and from 1 to 0 as shown in the figure. Namely, they show 12 changes in total with each A-electrode showing three changes.

[0077] Figure 12C shows a scan sequence that scans the Y-electrodes in order of Y1, Y3, Y2, and Y4. In this case, the A-electrodes A1 to A4 show four changes in total with each A-electrode showing one change.

[0078] When displaying the checkered pattern of Fig. 12A, the scan sequence of Fig. 12C greatly reduces the power consumption of a driver for driving the A-electrodes compared with the scan sequence of Fig. 12B.

[0079] Figure 13A shows another checkered pattern displayed on the same display as that of Fig. 12A.

[0080] Figure 13B shows a scan sequence that scans the Y-electrodes in order of Y1, Y2, Y3, and Y4. In this case, the A-electrodes A1 to A4 show four changes in total with each A-electrode showing one change.

[0081] Figure 13C shows a scan sequence that scans the Y-electrodes in order of Y1, Y3, Y2, and Y4. In this case, the A-electrodes A1 to A4 show 12 changes with each A-electrode showing three changes.

[0082] When displaying the checkered pattern of Fig. 13A, the scan sequence of Fig. 13B greatly reduces the power consumption of the driver for driving the A-electrodes compared with the scan sequence of Fig. 13C.

[0083] Figure 14 shows a "16 x 16" matrix of 256 cells (pixels) having Y-electrodes Y1 to Y16 and A-electrodes A1 to A16. The matrix displays stripes that alternate line by line. A normal scan sequence of Y1, Y2, Y3, Y4, ..., Y15, and Y16 causes 240 changes in total in the levels of the A-electrodes A1 to A16. An odd-even scan sequence of Y1, Y3, Y5, Y7, ..., Y15, and then, Y2, Y4, Y6, Y8, ..., Y14, and Y16 causes 16 changes in total in the levels of the A-addresses A1 to A16. Consequently, the odd-even scan sequence greatly reduces the power and current consumption of a driver for driving the A-electrodes.

[0084] Figure 15 shows a checkered pattern displayed on the same display as that of Fig. 14. The normal scan sequence mentioned above causes 240 changes in total in the levels of the A-electrodes A1 to A16, and the odd-even scan sequence mentioned above 16 changes. Consequently, the odd-even scan sequence can greatly reduce the power and current consumption of the driver for driving the A-electrodes.

[0085] Figure 16 shows a pattern displayed on the same display as that of Fig. 14. The normal scan sequence mentioned above causes 121 changes in total in the levels of the A-electrodes A1 to A16, and the odd-even scan sequence mentioned above 61 changes. Consequently, the odd-even scan sequence can greatly reduce the power and current consumption of the driver for driving the A-electrodes. In addition to the normal and odd-even scan sequences explained with reference to Figs. 14 to 16, a variety of scan sequences are possible according to an embodiment of the present invention.

[0086] Figure 17 is a block diagram showing a display according to the second embodiment of the present invention. The display has a panel 51, an address driver (A-driver) 52, a Y-driver 53, a counter 54, a sequential address generator 551, a 1-line-jump address generator 552, a 3-line-jump address generator 553, an address selector 554, a sequential scan sequencer 561, a 1-line-jump scan sequencer 562, a 3-line-jump scan sequencer 563, a scan selector 564, a memory 57, a detector 581, a controller 582, and a reference setter 583.

[0087] The A-driver 52, Y-driver 53, and memory 57 correspond to the address driver 23, Y-driver 24, and frame memory 29 of Fig. 4. The sequential scan generator 561, 1-line-jump scan sequencer 562, 3-line-jump scan sequencer 563, and scan selector 564 are installed in the scan driver controller 21 of Fig. 4. The counter 54, sequential address generator 551, 1-line-jump address generator 552, 3-line-jump address generator 553, address selector 554, detector 581, controller 582, and reference setter 583 are installed in the display data controller 28 of Fig. 4.

[0088] The display of the second embodiment is characterized by the sequential address generator 551, 1-line-jump address generator 552, 3-line-jump address generator 553, sequential scan sequencer 561, 1-line-jump scan sequencer 562, and 3-line-jump scan sequencer 563 that select one of three scan sequences to minimize the current and power consumption of the A-driver 52. Although the second embodiment uses sequential, 1-line-jump, and 3-line-jump scan sequences each of which is a power of 2, other embodiments of the present invention may employ address generators and scan sequencers that realize 7-line-jump, 15-line-jump, or any other sequences. The panel 51 of Fig. 17 has 1024 Y-electrodes Y1 to Y1024 and 1280 addressing electrodes (A-electrodes) A1 to A1280.

[0089] The detector 581 detects the current or power consumption of the A-driver 52 in response to the outputs of the sequential address generator 551, 1-line-

jump address generator 552, and 3-line-jump address generator 553. The address selector 554 selects one of the outputs of the address generators 551 to 553 that is determined to be the smallest by the detector 581. At the same time, the scan selector 564 selects one of the sequencers 561 to 563 that corresponds to the output selected by the address selector 554.

[0090] For example, if the detector 581 determines that the output of the sequential address generator 551 minimizes a current flowing through the A-driver 52, the address selector 554 selects the output of the sequential address generator 551, and the scan selector 564 selects the output of the sequential scan sequencer 561. If the output of the 1-line-jump address generator 552 is determined to minimize a current flowing through the A-driver 52, the address selector 554 selects the output of the 1-line-jump address generator 552, and the scan selector 564 selects the output of the 1-line-jump scan sequencer 562. If the output of the 3-line-jump address generator 553 is determined to minimize a current flowing through the A-driver 52, the address selector 554 selects the output of the 3-line-jump address generator 553, and the scan selector 564 selects the output of the 3-line-jump scan sequencer 563.

[0091] The reference setter 583 sets a reference value of a current (power) flowing through the A-driver 52. If an actual current flowing through the A-driver 52 is smaller than the reference value, the present scan sequence is maintained, and if not, the present scan sequence is changed to the output of another scan sequencer that brings the current below the reference value. The reference value is set in consideration of various display patterns so that at least one of the outputs of the scan sequencers 561 to 563 may bring an actual current passing through the A-driver 52 below the reference value.

[0092] A sequential scan set by the sequential scan sequencer 561 sequentially scans the Y-electrodes in order of Y1, Y2, Y3, Y4, ..., Y1023, and Y1024. One-line-jump scan set by the 1-line-jump scan sequencer 562 scans, for example, odd Y-electrodes and then even Y-electrodes in order of Y1, Y3, Y5, Y7, ..., Y1021, and Y1023, and then, Y2, Y4, Y6, Y8, ..., Y1022, and Y1024.

[0093] Figure 18 is a timing chart showing 3-line-jump scan set by the 3-line-jump scan sequencer 563.

[0094] This sequence scans the Y-electrodes in order of Y1, Y5, Y9, Y13, ..., Y1017, and Y1021, then, Y2, Y6, Y10, Y14, ..., Y1018, and Y1022, then, Y3, Y7, Y11, Y15, ..., Y1019, and Y1023, and then, Y4, Y8, Y12, Y16, ..., Y1020, and Y1024. For every Y-electrode to be scanned, the A-driver 52 applies proper display data to the A-electrodes A1 to A1280.

[0095] Figure 19 shows the operation of the sequential address generator 551, Fig. 20 the operation of the 1-line-jump address generator 552, and Fig. 21 the operation of the 3-line-jump address generator 553. In Figs. 19 to 21, 10 bits SLC0 to SLC9 are provided by the counter 54 for the 1024 Y-electrodes Y1 to Y1024. There are address signals address0, address1, and the like.

[0096] In Fig. 19, the Y-electrodes Y1 to Y1024 are sequentially scanned in order of Y1, Y2, Y3, Y4, ..., Y1023, and Y1024. The sequential address generator 551 uses the output signals SLC0 to SLC9 as they are to prepare the address signals address0 to address9. Higher address bits address10, adress11, and the like are determined according to sub-frame information, etc.

[0097] In Fig. 20, the Y-electrodes Y1 to Y1024 are scanned in odd-even order of Y1, Y3, Y5, Y7, ..., Y1021, and Y1023, and then, Y2, Y4, Y6, Y8, ..., Y1022, and Y1024. The 1-line-jump address generator 552 uses the output signals SLC0 to SLC8 to prepare the address signals address1 to address9, and the output signal SLC9 the address signal address0.

[0098] In Fig. 21, the Y-electrodes Y1 to Y1024 are scanned in order of Y1, Y5, Y9, Y13, ..., Y1017, and Y1021, then, Y2, Y6, Y10, Y14, ..., Y1018, and Y1022, then, Y3, Y7, Y11, Y15, ..., Y1019, and Y1023, and them, Y4, Y8, Y12, Y16, ..., Y1020, and Y1024. The 3-line-jump address generator 553 uses the output signals SLC0 to SLC7 to prepare the address signals address2 to address9, and the output signals SLC8 and SLC9 to prepare the address signals address0 and address1.

[0099] Figure 22 is a block diagram showing a display according to the third embodiment of the present invention. The display has a panel 61, an address driver (A-driver) 62, a Y-driver 63, a counter 64, an address generator 65, a decoder 66, a memory 67, a difference detector circuit 681, and a controller 682.

[0100] The A-driver 62, Y-driver 63, and memory 67 correspond to the address driver 23, Y-driver 24, and frame memory 29 of Fig. 4. The decoder 66 is installed in the scan driver controller 21 of Fig. 4. The difference detector circuit 681, controller 682, counter 64, and address generator 65 are installed in the display data controller 28 of Fig. 4.

[0101] The display of the third embodiment is characterized in that the controller 682 is capable of optionally specifying a scan sequence. Display data is supplied to the difference detector circuit 681, which detects the difference between display data for a scan start line and display data for each of the other lines. Here, the lines correspond to Y-electrodes. The controller 682 determines a scan sequence so that the lines are scanned in ascending order of the differences between the scan start line and the other lines. Namely, EXORs are calculated among the display data for the lines, and any line involving a smaller number of 1s is scanned earlier.

[0102] According to the scan sequence determined by the controller 682, the decoder 66 selects a line to scan, and the address generator 65 outputs corresponding address signals. The panel 61 may be divided into blocks each having a predetermined number (for example, 4 or 8) of lines, to simplify the structure of Fig. 22.

[0103] Figure 23 is a block diagram showing a display according to the fourth embodiment of the present invention. This embodiment is based on the third embodiment of Fig. 22. A matrix panel 71 is divided into blocks in a scanning direction with each block containing four lines, i.e., four Y-electrodes. In each block, a scan sequence of the four lines is optimized.

[0104] The display of Fig. 23 has the panel 71, an address driver (A-driver) 72, a Y-driver 73, a scan counter 74, an address generator 75, a scan sequencer 76, a memory 77, a difference detector circuit 781, a controller 782, and a scan sequence memory 783.

[0105] The A-driver 72, Y-driver 73, and memory 77 correspond to the address driver 23, Y-driver 24, and frame memory 29 of Fig. 4. The scan sequencer 76 is installed in the scan driver controller 21 of Fig. 4. The difference detector circuit 781, controller 782, scan sequence memory 783, scan counter 74, and address generator 75 are installed in the display data controller 28 of Fig. 4.

[0106] Figure 24 is a block diagram showing an example of the difference detector circuit 781.

[0107] The difference detector circuit 781 consists of four line memories 701 to 704 for storing display data for four consecutive lines, difference detectors 710 to 740 for detecting the differences between input display data and the display data stored in the line memories 701 to 704, and latches 711 to 714, 721 to 723, 731, 732, and 741 for latching the outputs of the difference detectors 710 to 740 in response to latch control signals (strobe signals) L0 to L3.

[0108] The line memories 701 to 704 receive display data for four consecutive lines and store them. The output of the difference detector 710 is latched by the four latches 711 to 714 in response to the latch control signals L0 to L3 each having different timing. The output of the difference detector 720 is latched by the three latches 721 to 723 in response to the latch control signals L1 to L3. The output of the difference detector 730 is latched by the two latches 731 and 732 in response to the latch control signals L2 and L3. The output of the difference detector 740 is latched by the latch circuit 741 in response to the latch control signal L3.

[0109] Figure 25 is a block diagram showing an example of the difference detector 710. The other difference detectors 720 to 740 have each the same structure as the difference detector 710.

[0110] The difference detector 710 has an exclusive OR (EXOR) circuit 7101 and a counter 7102 to count the number of unequal bits between input display data (a) for one line and the output (b) of the line memory 701.

[0111] Figure 26 shows a circuit for generating the latch control signals L0 to L3.

[0112] The latch signal generator 750 consists of a 2-bit counter 751 for receiving a horizontal synchronizing signal HSYNC and a 2-to-4 decoder 752 for converting a 2-bit signal into a 4-bit signal. Each of the latch control signals L0 to L3 is provided once in a period in which four lines are scanned. The signals L0 to L3 are shifted from one another by a one-line-scan period as shown in Fig. 27.

[0113] Figure 27 is a timing chart showing the operation of the difference detector circuit 781.

[0114] The operations of the difference detector circuit 781 and display of the fourth embodiment will be explained with reference to Fig. 27.

[0115] The outputs of the difference detectors 710 to 740 are latched by the latches 711 to 714, 721 to 723, 731, 732, and 741 in response to the latch control signals L0 to L3. Here, a line "P" represents display data for the last line scanned in a block preceding a target block. The differences between the display data for the line P and display data for four lines 1 to 4 of the target block are detected, and one among the lines 1 to 4 that provides the smallest difference with respect to the line P will be the first scan line in the target block.

[0116] Once the first scan line in the target block is determined, one among the remaining three lines that has the smallest difference in display data with respect to the first scan line is selected as the second scan line. Similarly, a line having the smallest difference in display data with respect to the second scan line is selected as the third scan line. Then, the fourth scan line is determined. These processes are carried out on every block of display lines on the panel 71, to determine a scan sequence of four lines in every block. The scan sequences thus determined to cover all lines are stored in the scan sequence memory 783.

[0117] In Fig. 27, display data for the lines P, 1, 2, 3, and 4 are sequentially input. The line memory 701 delays these data pieces by one line period each time, i.e., one horizontal synchronizing period and outputs them one after another. The line memory 702 delays the data pieces by two line periods each time and outputs them one after another. The line memory 703 delays the data pieces by three line periods each time and outputs them one after another. The line memory 704 delays the data pieces by four line periods each time and outputs them one after another.

[0118] The input display data and the outputs of the line memories 701 to 704 are supplied to the difference detectors 710 to 740, which count and output unequal bits as explained with reference to Fig. 25. The outputs of the difference detectors 710 to 740 are latched by the latches 711 to 714, 721 to 723, 731, 732, and 741 in response to the latch control signals L0 to L3. More precisely, the latch 711 latches the difference in display data between the lines P and 1 in response to the latch control signal L0. Here, the line P is the last line scanned in the preceding block, and the line 1 is the first line scanned in the target block. The latch circuit 712 latches the difference in display data between the lines 1 and 2 in the target block in response to the latch control signal L1. The latch circuit 713 latches the difference in display data between the lines 2 and 3 in the

target block in response to the latch control signal L2. The latch circuit 714 latches the difference in display data between the lines 3 and 4 in the target block in response to the latch control signal L3.

[0119] Similarly, the latch circuit 721 latches the difference in display data between the lines P and 2 in response to the latch control signal L1. The latch circuit 722 latches the difference in display data between the lines 1 and 3 in response to the latch control signal L2. The latch circuit 723 latches the difference in display data between the lines 2 and 4 in response to the latch control signal L3. In this way, the difference in display data between optional two of the lines P and 1 to 4 is detected and evaluated to determine a scan sequence that minimizes current and power consumption. After a scan sequence of four lines in every block is determined, the determined scan sequences that cover all lines are stored in the scan sequence memory 783.

[0120] The controller 782 reads the scan sequences out of the memory 783 and controls the scan sequencer 76 and address generator 75, to scan the Y-electrodes through the Y-driver 73 according to the scan sequences. At the same time, the controller 782 provides the A-electrodes with proper display data through the memory 77 and A-driver 72 according to the scan sequences.

[0121] Figure 28 is a block diagram showing an example of the scan sequencer 76 of Fig. 23.

[0122] The scan sequencer 76 has a 2-to-4 decoder 761 for converting a 2-bit signal into a 4-bit signal, a 256-stage shift register 762, a 1/4 frequency divider 763 for quartering the frequency of the scan clock signal SCLOCK, i.e. quadrupling the period of the signal SCLOCK, and AND circuits 764 to 767 for providing ANDs of the output signals sel0 to sel3 of the decoder 761 and the outputs of the shift register 762 for each block. The 1024 Y-electrodes Y1 to Y1024 are divided into 256 blocks each containing four Y-electrodes. Accordingly, the shift register 762 sequentially scans the 256 blocks at the 1/4 frequency of the scan clock signal SCLOCK.

[0123] When a block is scanned by the shift register 762, the scanning sequence of four lines of the block is controlled according to the four control signals sel0 to sel3 that are prepared by decoding control signals CNT0 and CNT1 provided by the controller 782. At this time, the scanning sequence of four lines of each block is determined to minimize the current and power consumption of the A-driver 72.

[0124] Figure 29 shows the operation of the address generator 75 of Fig. 23.

[0125] The address generator 75 uses output signals SLC2 to SLC9 of the scan counter 74 as they are to provide address signals address2 to address9, and uses the control signals CNT0 and CNT1 from the controller 782 to prepare address signals address0 and address1. Output signals SLC0 and SLC1 of the scan counter 74 are not used.

[0126] As a result, the A-driver 72 provides the addressing electrodes A1 to A1280 with display data corresponding to one of the Y-electrodes Y1 to Y1024 selected by the scan sequencer 76.

[0127] The embodiments mentioned above may be combined in various ways. Although the embodiments relate to 3-electrode, surface-discharge AC PDP displays, embodiments of the present invention are applicable to a variety of matrix-electrode-scanning displays such as PDP displays, EL displays, LCDs, VFDs, and LED displays.

[0128] As explained above, the displays and display driving methods of embodiments of the present invention are capable of reducing the current and power consumption of an address driver without deteriorating the quality of images to display.

[0129] Many different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention, and it should be understood that the present invention is not limited to the specific embodiments described in this specification, except as defined in the appended claims.

Claims

1. A display having a panel, and first and second electrodes; said first and second electrodes defining a matrix of cells on said panel; said second electrodes, which correspond to lines of said cells, being scanned to select cell lines one by one; said first electrodes being driven to set display data for a selected one of said cell lines, wherein said display comprises:

   a sequence setting unit for setting sequences of scanning said second electrodes; and
   a sequence selection unit for selecting one of the sequences.

2. A display as claimed in claim 1, wherein said display further comprises:

   a difference detection unit for detecting differences between display data set for said cell lines so that one of the sequences that minimizes the differences is selected.

3. A display as claimed in claim 1, wherein said display further comprises:

   a difference detection unit for detecting differences between display data set for said cell lines; and
   an upper limit setting unit for setting an upper limit so that one of the sequences that suppresses the differences to below the upper limit is selected.

4. A display as claimed in any preceding claim, wherein the sequences are set based on powers of two.

5. A display as claimed in any preceding claim, wherein:

   said sequence setting unit divides said second electrodes into blocks and sets sequences of scanning said second electrodes block by block; and
   said sequence selection unit selects one of the sequences in each of said blocks.

6. A display as claimed in any preceding claim, wherein said first electrodes are addressing electrodes, and said second electrodes are scan electrodes.

7. A display as claimed in claim 6, wherein said display further comprises:

   an address driver for driving said addressing electrodes;
   a current/power value detection unit for detecting a current or power value of said address driver; and
   a sequence changing unit for changing a sequence of scanning said second electrodes to minimize the current or power value.

8. A display as claimed in claim 7, wherein said display further comprises:

   a current/power value evaluation unit for evaluating a current or power value of said address driver according to display data set for said cell lines so that one of the sequences that minimizes the current or power value is selected.

9. A display as claimed in claim 7, wherein said display further comprises:

   a reference value setting unit for setting a reference value so that one of the sequences that suppresses the current or power value to below the reference value is selected.

10. A display as claimed in claim 7, wherein said display further comprises:

   a current/power value evaluation unit for evaluating a current or power value of said address driver according to display data set for said cell lines; and
   a reference value setting unit for setting a reference value so that one of the sequences that suppresses the current or power value to below the reference value is selected.

11. A display as claimed in claim 7, wherein said display further comprises:

   a current/power value evaluation unit for evaluating a current or power value of said address driver beforehand according to display data set for said cell lines; and
   a reference value setting unit for setting a reference value so that one of the sequences that suppresses the current or power value to below the reference value is selected.

12. A display as claimed in any preceding claim, wherein said display further comprises:

   a display data supplying unit for supplying display data line by line to said first electrodes according to the selected sequence of scanning said second electrodes.

13. A display as claimed in any preceding claim, wherein said display is a plasma display; a frame of display data is divided into a plurality of sub-frames that are selectively combined to display gradations; and each of the sub-frames at least includes an addressing period and a sustain period.

14. A display as claimed in any preceding claim, wherein said panel is a three-electrode surface-discharge alternating-current plasma display panel having third electrodes that run in parallel with said second electrodes and applying an alternating voltage to said second and third electrodes to repeat a sustain discharge.

15. A display having a panel, and first and second electrodes; said first and second electrodes defining a matrix of cells on said panel; said second electrodes, which correspond to lines of said cells, being scanned to select cell lines one by one; said first electrodes being driven to set display data for a selected one of said cell lines, wherein said display comprises:

   a sequence setting unit for optionally setting a sequence of scanning said second electrodes.

16. A display as claimed in claim 15, wherein said display further comprises:

   a difference detection unit for detecting differences between display data set for said cell lines so that said second electrodes are scanned in a sequence to minimize the differences.

17. A display as claimed in claim 15, wherein said display further comprises:

a difference detection unit for detecting differences between display data set for said cell lines; and
an upper limit setting unit for setting an upper limit so that said second electrodes are scanned in a sequence to suppress the differences to below the upper limit.

18. A display as claimed in claim 15, 16 or 17, wherein said sequence setting unit divides said second electrodes into blocks and sets a sequence of scanning said second electrodes in each of said blocks.

19. A display as claimed in any one of claims 15 to 18, wherein said first electrodes are addressing electrodes, and said second electrodes are scan electrodes.

20. A display as claimed in claim 19, wherein said display further comprises:

an address driver for driving said addressing electrodes;
a current/power detection unit for detecting a current or power value of said address driver; and
a sequence changing unit for changing a sequence of scanning said second electrodes to minimize the current or power value.

21. A display as claimed in claim 20, wherein said display further comprises:

a current/power evaluation unit for evaluating a current or power value of said address driver according to display data set for said cell lines so that said second electrodes are scanned in a sequence to minimize the current or power value.

22. A display as claimed in claim 20, wherein said display further comprises:

a reference value setting unit for setting a reference value so that said second electrodes are scanned in a sequence to suppress the current or power value to below the reference value.

23. A display as claimed in claim 20, wherein said display further comprises:

a current/power evaluation unit for evaluating a current or power value of said address driver according to display data set for said cell lines; and
a reference value setting unit for setting a reference value so that said second electrodes are scanned in a sequence to suppress the current or power value to below the reference value.

24. A display as claimed in claim 20, wherein said display further comprises:

a current/power evaluation unit for evaluating a current or power value of said address driver beforehand according to display data set for said cell lines; and
a reference value setting unit for setting a reference value so that said second electrodes are scanned in a sequence to suppress the current or power value to below the reference value.

25. A display as claimed in any one of claims 15 to 24, wherein said display further comprises:

a display data supplying unit for supplying display data line by line to said first electrodes according to the determined sequence of scanning said second electrodes.

26. A display as claimed in any one of claims 15 to 25, wherein said display is a plasma display; a frame of display data is divided into a plurality of sub-frames that are selectively combined to display gradations; and each of the sub-frames at least includes an addressing period and a sustain period.

27. A display as claimed in any one of claims 15 to 26, wherein said panel is a three-electrode surface-discharge alternating-current plasma display panel having third electrodes that run in parallel with said second electrodes and applying an alternating voltage to said second and third electrodes to repeat a sustain discharge.

28. A method of driving a display having a panel, and addressing and scan electrodes, said addressing and scan electrodes defining a matrix of cells on said panel; said scan electrodes, which correspond to lines of said cells, being scanned to select said cell lines one by one; said addressing electrodes being driven to set display data for a selected one of said cell lines, wherein said method comprises the steps of:

setting sequences of scanning said scan electrodes;
detecting a current or power value of an address driver for driving said addressing electrodes; and
selecting one of the sequences in accordance with the detected current or power value.

29. A method of driving a display as claimed in claim 28, wherein the sequences are set based on powers of two.

30. A method of driving a display having a panel, and addressing and scan electrodes, said addressing and scan electrodes defining a matrix of cells on said panel; said scan electrodes, which correspond to lines of said cells, being scanned to select said cell lines one by one; said addressing electrodes being driven to set display data for a selected one of said cell lines, wherein said method comprises the steps of:

detecting a current or power value of an address driver for driving said addressing electrodes; and
optionally setting a sequence of scanning said scan electrodes in accordance with the detected current or power value.

31. A method of driving a display as claimed in claim 30, wherein said method further comprises the steps of:

dividing said scan electrodes into blocks; and
setting a sequence of scanning said scan electrodes in each of said blocks.

Fig.1

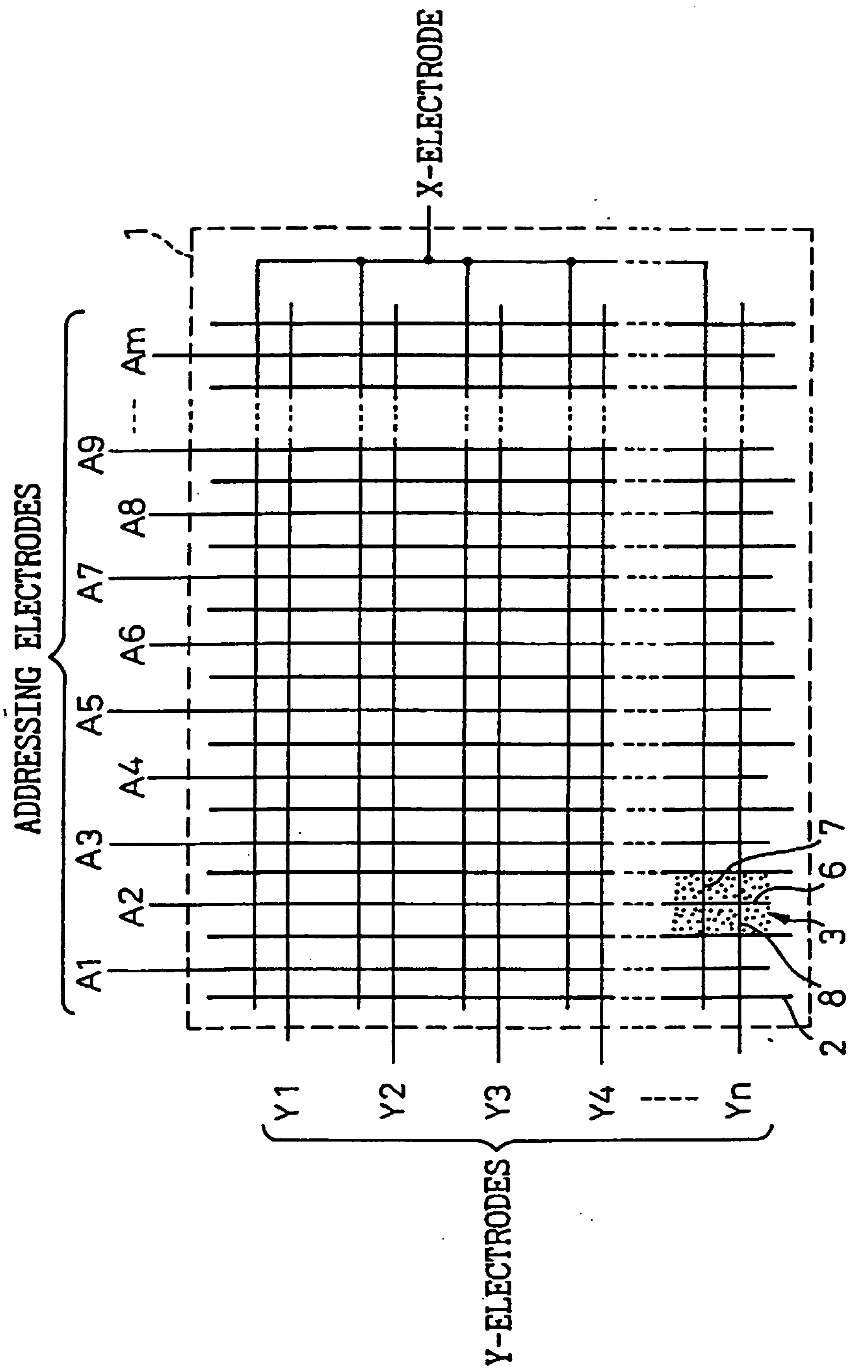

ADDRESSING ELECTRODES
A1
A2
A3
A4
A5
A6
A7
A8
A9
Am
X-ELECTRODE
1
2
3
6
7
8
Y1
Y2
Y3
Y4
Yn
Y-ELECTRODES

Fig.2

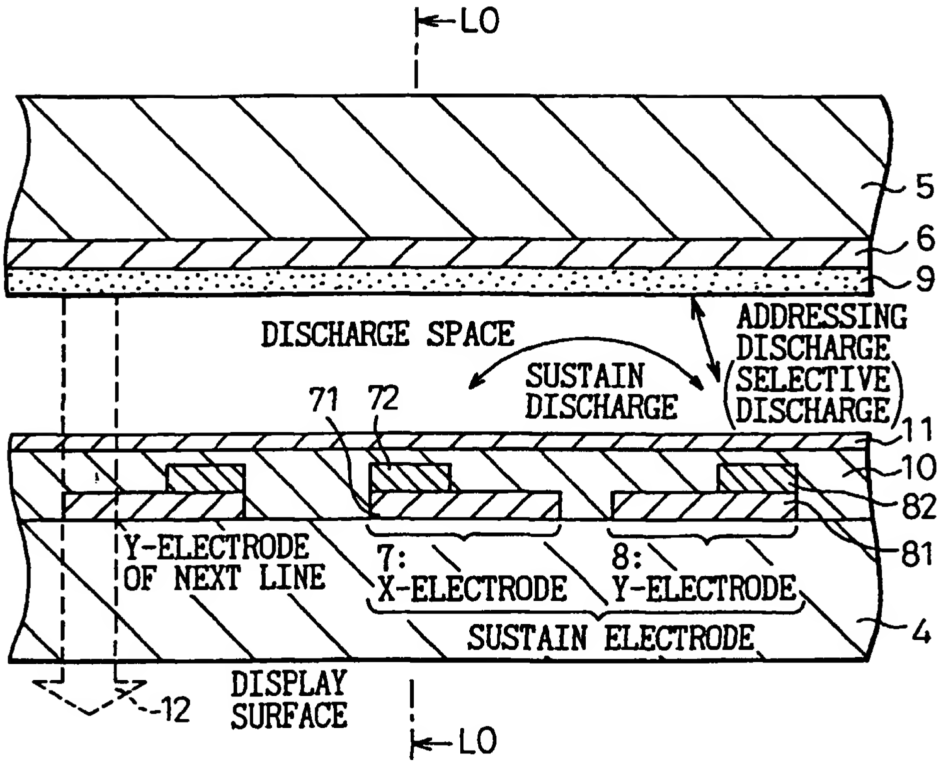

LO
5
6
9
DISCHARGE SPACE
ADDRESSING
DISCHARGE
(SELECTIVE
DISCHARGE)
SUSTAIN
DISCHARGE
71
72
11
10
82
81
Y-ELECTRODE
OF NEXT LINE
7:
X-ELECTRODE
8:
Y-ELECTRODE
SUSTAIN ELECTRODE
4
12
DISPLAY
SURFACE
LO

Fig. 3

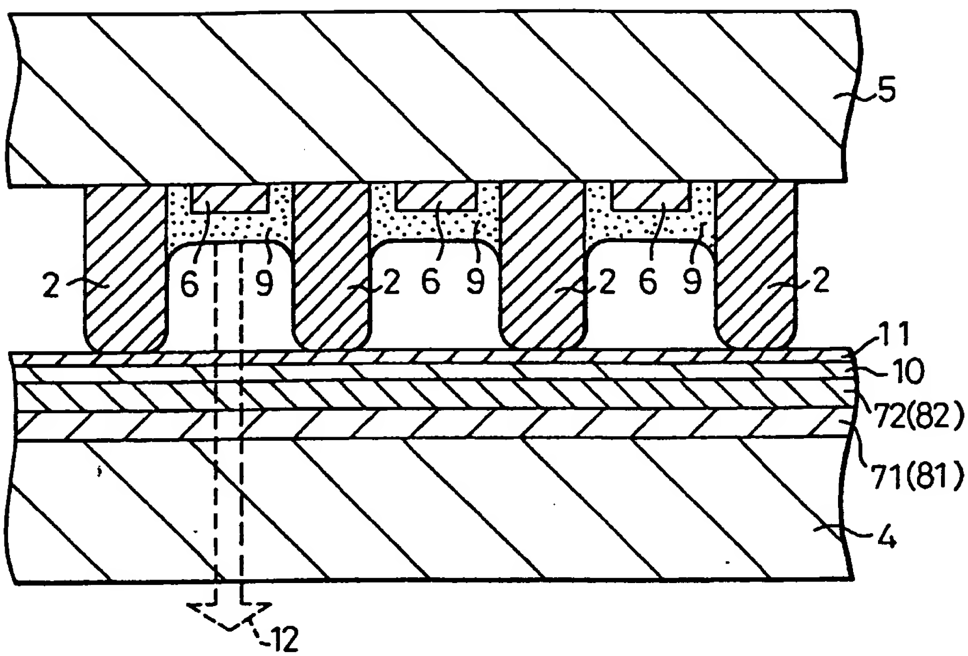


Fig. 4

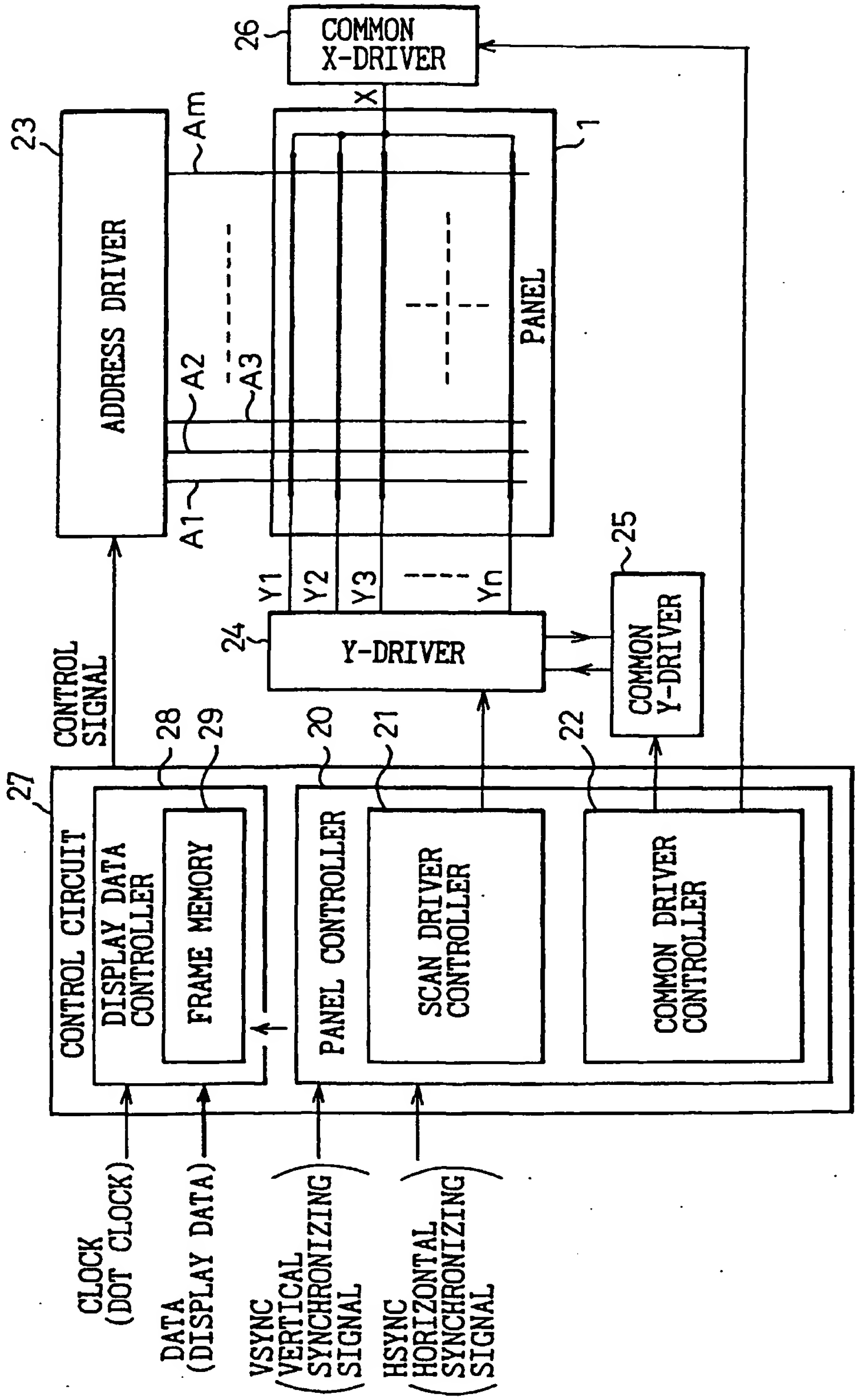

COMMON X-DRIVER
26
X
23
Am
ADDRESS DRIVER
A2
A3
A1
1
PANEL
Y1
Y2
Y3
Yn
24
Y-DRIVER
25
COMMON Y-DRIVER
CONTROL SIGNAL
28
29
20
21
22
27
CONTROL CIRCUIT
DISPLAY DATA CONTROLLER
FRAME MEMORY
PANEL CONTROLLER
SCAN DRIVER CONTROLLER
COMMON DRIVER CONTROLLER
CLOCK (DOT CLOCK)
DATA (DISPLAY DATA)
VSYNC (VERTICAL SYNCHRONIZING SIGNAL)
HSYNC (HORIZONTAL SYNCHRONIZING SIGNAL)

Fig.5

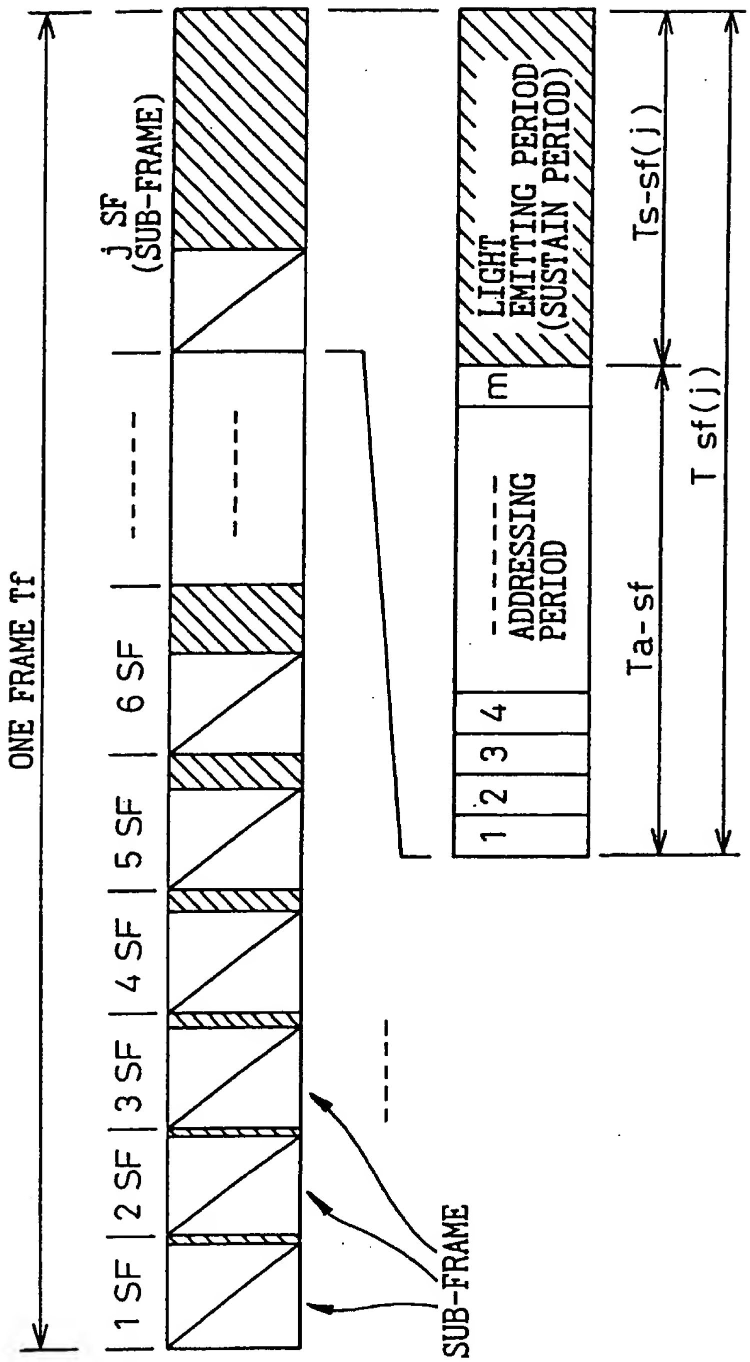
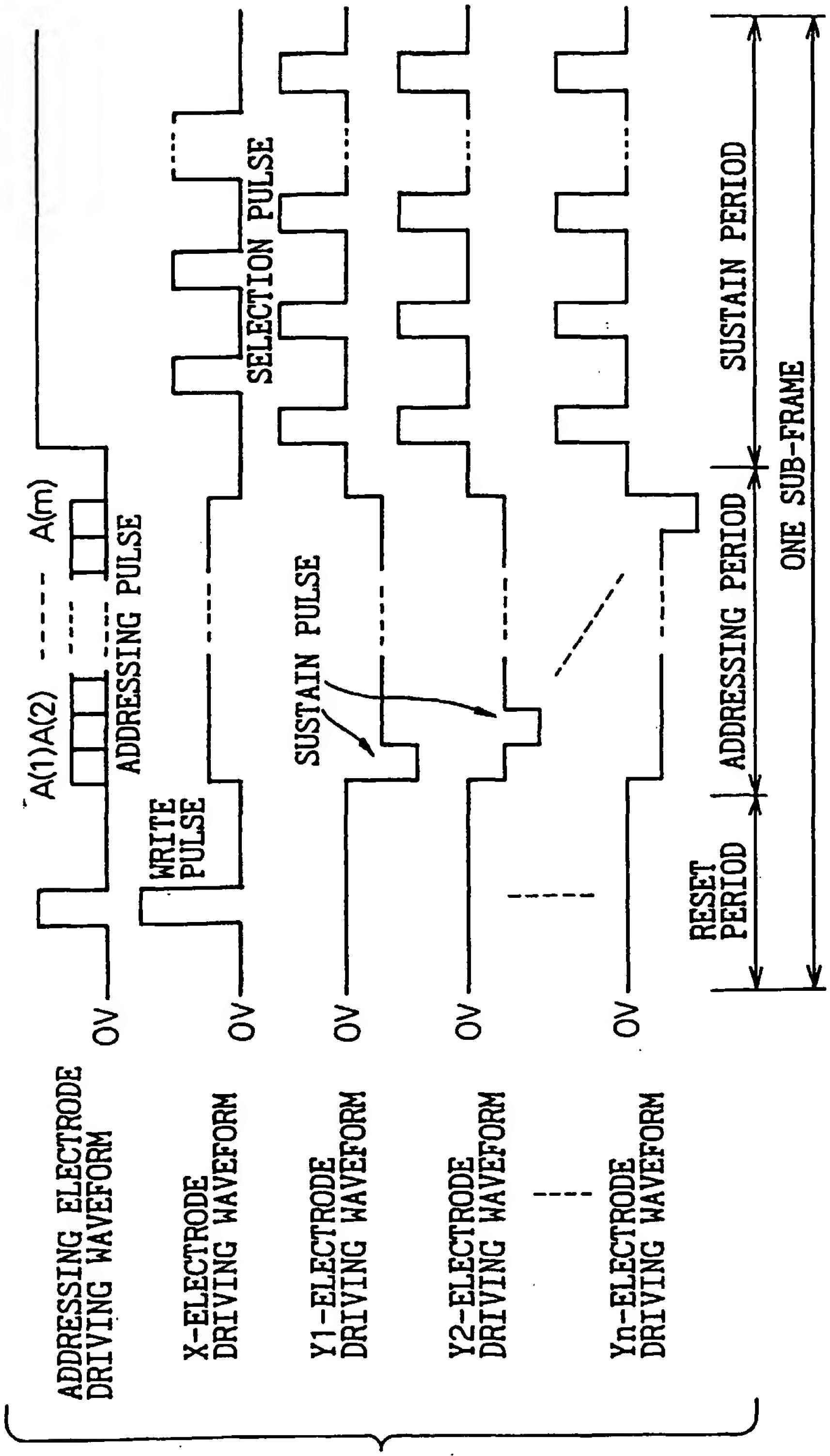

ONE FRAME Tf
1 SF
2 SF
3 SF
4 SF
5 SF
6 SF
j SF
(SUB-FRAME)
SUB-FRAME
1
2
3
4
ADDRESSING
PERIOD
m
LIGHT
EMITTING PERIOD
(SUSTAIN PERIOD)
Ta-sf
Ts-sf(j)
T sf(j)

Fig.6



ADDRESSING ELECTRODE DRIVING WAVEFORM
X-ELECTRODE DRIVING WAVEFORM
Y1-ELECTRODE DRIVING WAVEFORM
Y2-ELECTRODE DRIVING WAVEFORM
Yn-ELECTRODE DRIVING WAVEFORM
0V
0V
0V
0V
0V
A(1)A(2) ----- A(m)
ADDRESSING PULSE
WRITE PULSE
SELECTION PULSE
SUSTAIN PULSE
RESET PERIOD
ADDRESSING PERIOD
SUSTAIN PERIOD
ONE SUB-FRAME

Fig. 7

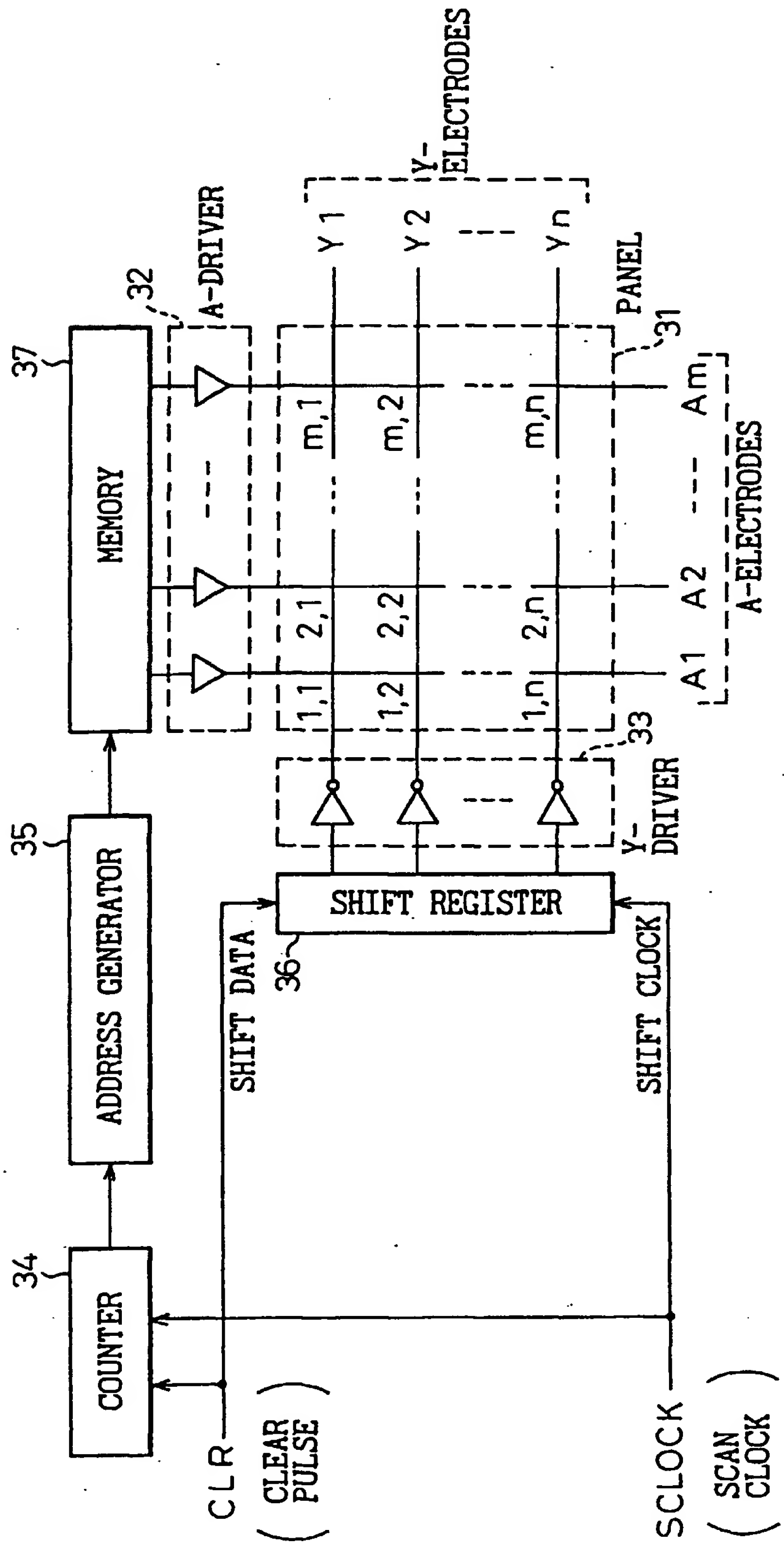

MEMORY
37
32
A-DRIVER
ADDRESS GENERATOR
35
COUNTER
34
Y-ELECTRODES
Y 1
Y 2
Y n
PANEL
31
m,1
m,2
m,n
2,1
2,2
2,n
1,1
1,2
1,n
A1
A2
Am
A-ELECTRODES
33
Y-DRIVER
SHIFT REGISTER
36
SHIFT DATA
SHIFT CLOCK
CLR
(CLEAR PULSE)
SCLOCK
(SCAN CLOCK)

Fig.8

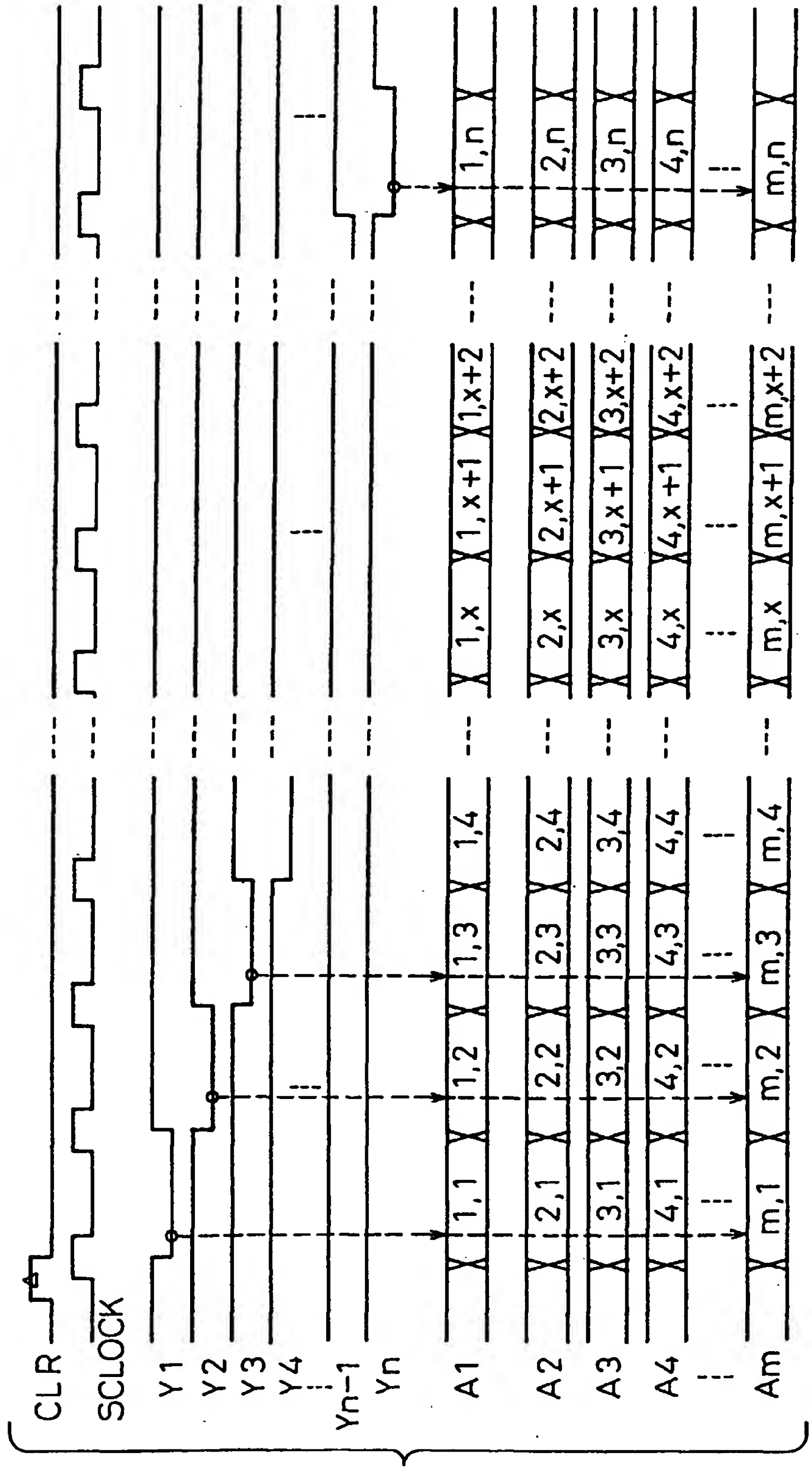

CLR
SCLOCK
Y1
Y2
Y3
Y4
Yn-1
Yn
A1
A2
A3
A4
Am
1,1
1,2
1,3
1,4
1,x
1,x+1
1,x+2
1,n
2,1
2,2
2,3
2,4
2,x
2,x+1
2,x+2
2,n
3,1
3,2
3,3
3,4
3,x
3,x+1
3,x+2
3,n
4,1
4,2
4,3
4,4
4,x
4,x+1
4,x+2
4,n
m,1
m,2
m,3
m,4
m,x
m,x+1
m,x+2
m,n

Fig.9

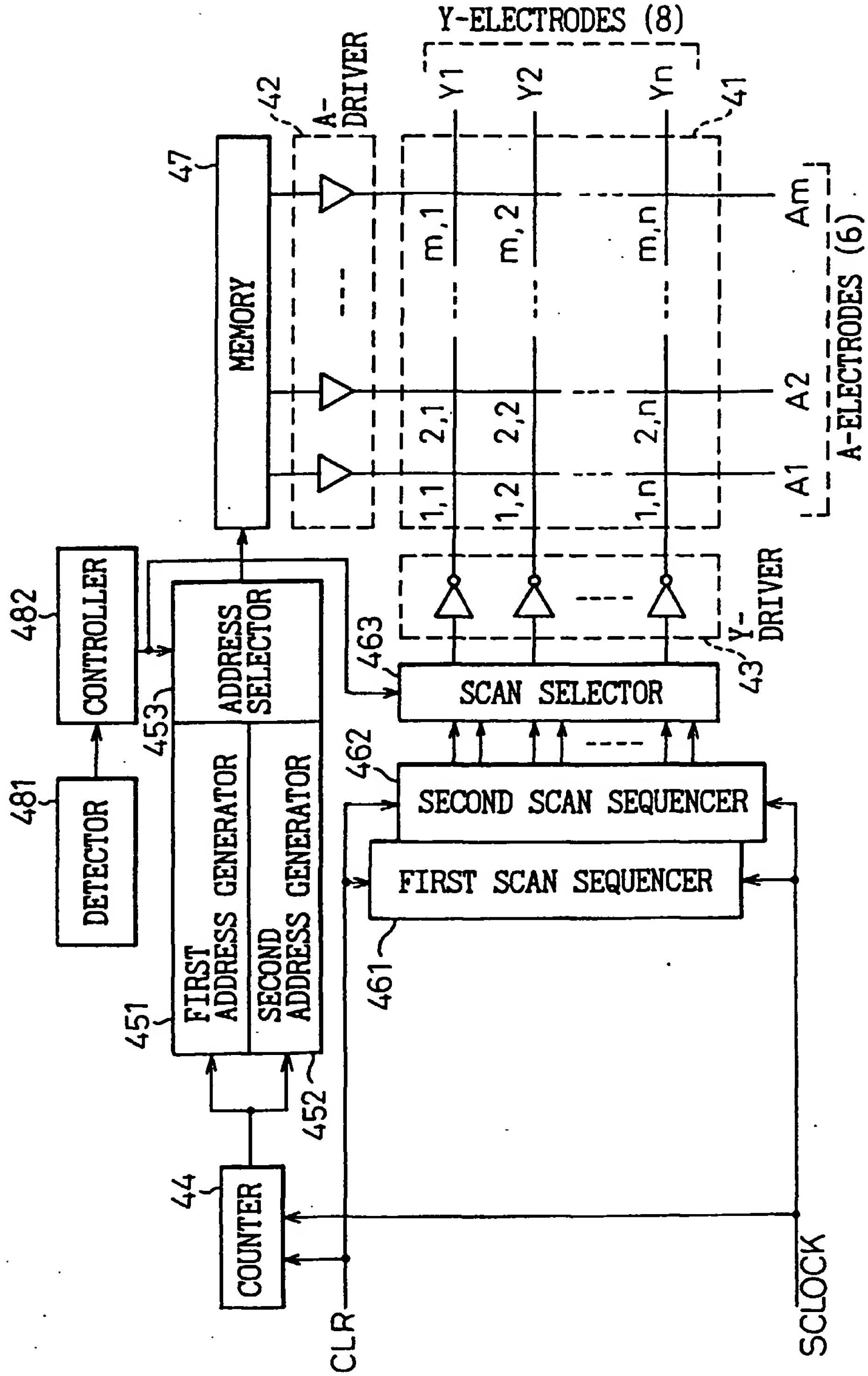

Y-ELECTRODES (8)
Y1
Y2
Yn
41
42
A-DRIVER
47
MEMORY
Am
A2
A1
A-ELECTRODES (6)
m,1
m,2
m,n
2,1
2,2
2,n
1,1
1,2
1,n
Y-DRIVER
43
482
CONTROLLER
481
DETECTOR
ADDRESS SELECTOR
453
463
SCAN SELECTOR
462
SECOND SCAN SEQUENCER
FIRST SCAN SEQUENCER
461
451
FIRST ADDRESS GENERATOR
SECOND ADDRESS GENERATOR
452
44
COUNTER
CLR
SCLOCK

Fig.10

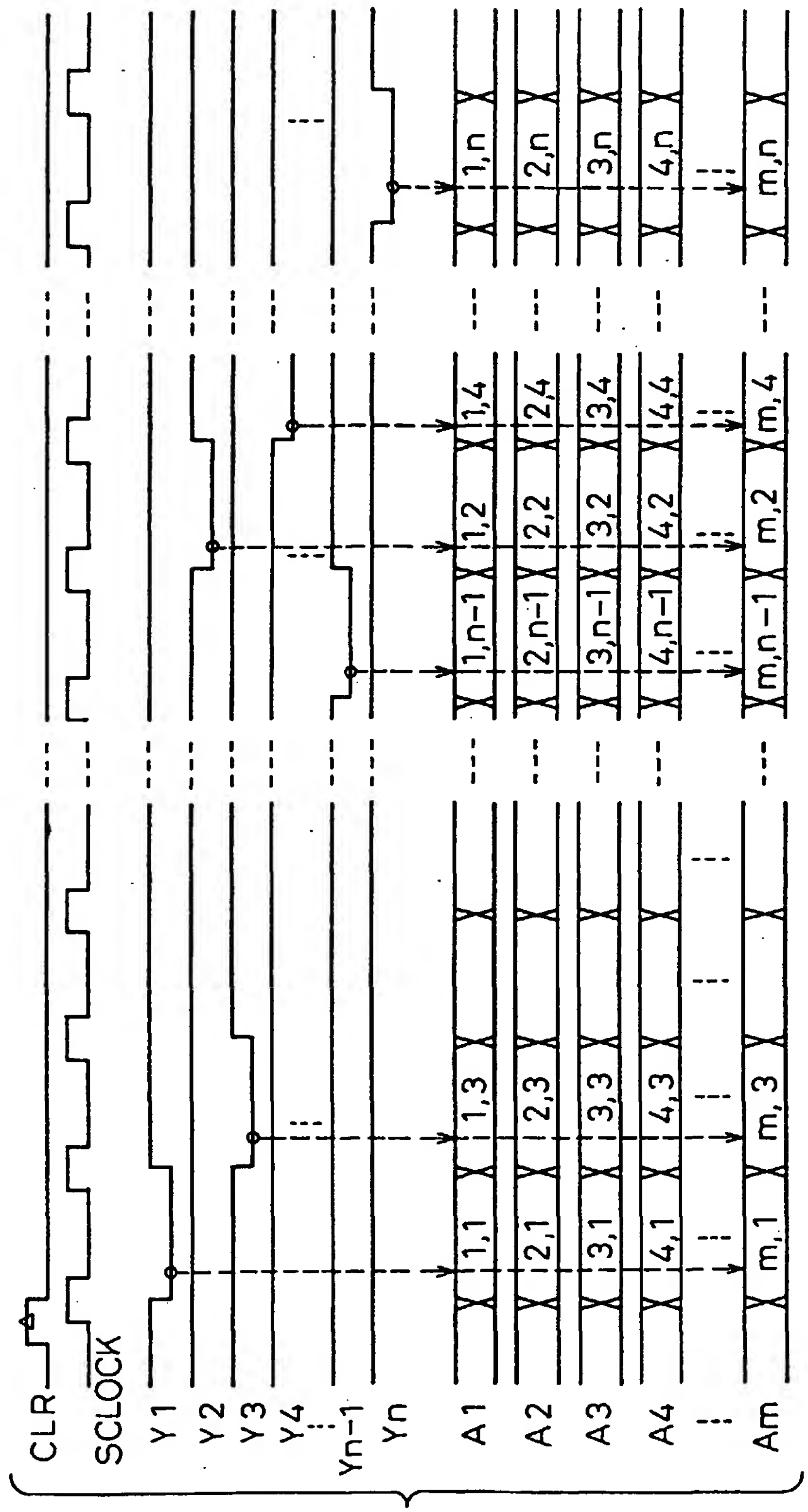
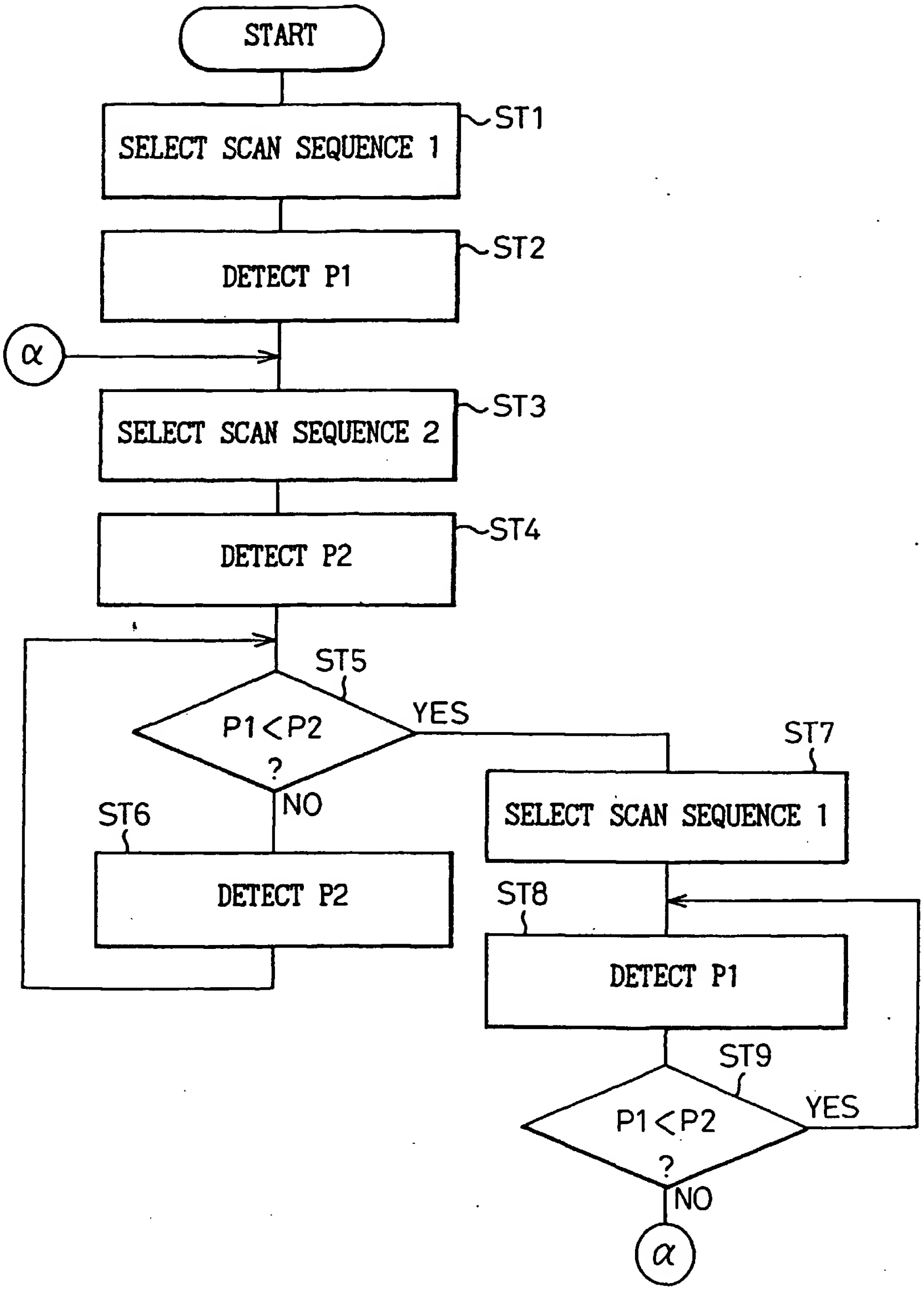

CLR
SCLOCK
Y1
Y2
Y3
Y4
Yn-1
Yn
A1
A2
A3
A4
Am
1,1
2,1
3,1
4,1
m,1
1,3
2,3
3,3
4,3
m,3
1,n-1
2,n-1
3,n-1
4,n-1
m,n-1
1,2
2,2
3,2
4,2
m,2
1,4
2,4
3,4
4,4
m,4
1,n
2,n
3,n
4,n
m,n

Fig.11


START
SELECT SCAN SEQUENCE 1
ST1
DETECT P1
ST2
α
SELECT SCAN SEQUENCE 2
ST3
DETECT P2
ST4
ST5
P1<P2 ?
YES
NO
ST6
DETECT P2
ST7
SELECT SCAN SEQUENCE 1
ST8
DETECT P1
ST9
P1<P2 ?
YES
NO
α

[CHECKERED PATTERN]

DATA (DISPLAY PATTERN)

Fig.12A

	A1	A2	A3	A4
Y1	1	0	1	0
Y2	0	1	0	1
Y3	1	0	1	0
Y4	0	1	0	1

Fig.12B

CHANGES IN A-ELECTRODES
IN SCAN SEQUENCE 1

	SCAN SEQUENCE Y1 → Y2 → Y3 → Y4	CHANGES
A1	1 → 0 → 1 → 0	3
A2	0 → 1 → 0 → 1	3
A3	1 → 0 → 1 → 0	3
A4	0 → 1 → 0 → 1	3
	TOTAL	12

Fig.12C

CHANGES IN A-ELECTRODES
IN SCAN SEQUENCE 2

	SCAN SEQUENCE Y1 → Y3 → Y2 → Y4	CHANGES
A1	1 → 1 → 0 → 0	1
A2	0 → 0 → 1 → 1	1
A3	1 → 1 → 0 → 0	1
A4	0 → 0 → 1 → 1	1
	TOTAL	4

[TWO-LINE CHECKERED PATTERN]

DATA (DISPLAY PATTERN)

Fig.13A

	A1	A2	A3	A4
Y1	1	0	1	0
Y2	1	0	1	0
Y3	0	1	0	1
Y4	0	1	0	1

CHANGES IN A-ELECTRODES
IN SCAN SEQUENCE 1

Fig.13B

	SCAN SEQUENCE Y1 → Y2 → Y3 → Y4	CHANGES
A1	1 → 1 → 0 → 0	1
A2	0 → 0 → 1 → 1	1
A3	1 → 1 → 0 → 0	1
A4	0 → 0 → 1 → 1	1
	TOTAL	4

CHANGES IN A-ELECTRODES
IN SCAN SEQUENCE 2

Fig.13C

	SCAN SEQUENCE Y1 → Y3 → Y2 → Y4	CHANGES
A1	1 → 0 → 1 → 0	3
A2	0 → 1 → 0 → 1	3
A3	1 → 0 → 1 → 0	3
A4	0 → 1 → 0 → 1	3
	TOTAL	12

Fig.14

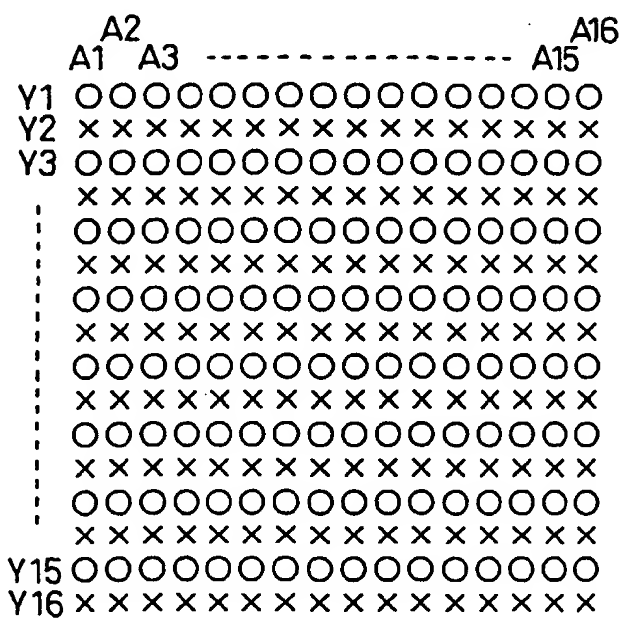


Fig.15

	A1	A2	A3												A15	A16
Y1	O	O	O	×	×	×	O	O	O	×	×	×	O	O	O	×
Y2	×	×	×	O	O	O	×	×	×	O	O	O	×	×	×	O
Y3	O	O	O	×	×	×	O	O	O	×	×	×	O	O	O	×
	×	×	×	O	O	O	×	×	×	O	O	O	×	×	×	O
	O	O	O	×	×	×	O	O	O	×	×	×	O	O	O	×
	×	×	×	O	O	O	×	×	×	O	O	O	×	×	×	O
	O	O	O	×	×	×	O	O	O	×	×	×	O	O	O	×
	×	×	×	O	O	O	×	×	×	O	O	O	×	×	×	O
	O	O	O	×	×	×	O	O	O	×	×	×	O	O	O	×
	×	×	×	O	O	O	×	×	×	O	O	O	×	×	×	O
	O	O	O	×	×	×	O	O	O	×	×	×	O	O	O	×
	×	×	×	O	O	O	×	×	×	O	O	O	×	×	×	O
	O	O	O	×	×	×	O	O	O	×	×	×	O	O	O	×
	×	×	×	O	O	O	×	×	×	O	O	O	×	×	×	O
Y15	O	O	O	×	×	×	O	O	O	×	×	×	O	O	O	×
Y16	×	×	×	O	O	O	×	×	×	O	O	O	×	×	×	O

Fig.16

A2 A16
A1 A3 --------------- A15

Y1 × × × O O × O O × O O × × × × ×
Y2 × × O × × O × × O × × O × O O ×
Y3 × × O × × O × × O × × O O × × O
× O O O O O O O O O O × O × × O
O × × × O × × × × × × O O O O ×
O × × O × × O O O O × × O × × O
× O O O × O × × × × O × O × × O
O × × O × O × O O × O × O O O ×
O × × O × O × O O × O × O × × O
× O O O × O × × × × O × O × × O
O × × O × × O O O O × × O O O ×
O × × O O × × × × × × O × × × O
× O O × O O O O O O O O O × × O
× × × O × × O × × O × × O O O ×
Y15 × × × O × × O × × O × × O × × ×
Y16 × × × × O O × O O × O O × × × ×

Fig.17

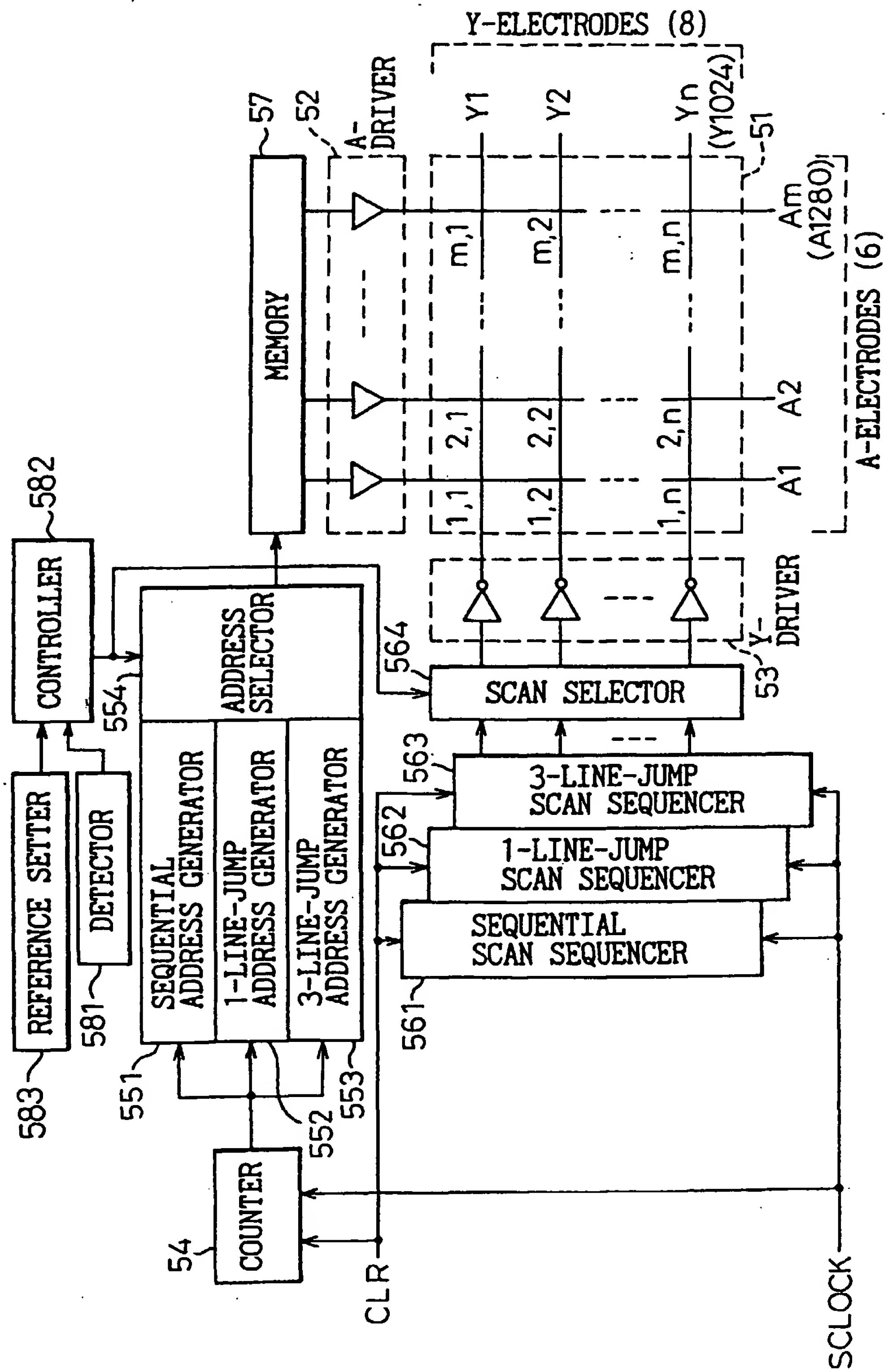

Y-ELECTRODES (8)
A-DRIVER
MEMORY
57
52
Y1
Y2
Yn
(Y1024)
51
Am
(A1280)
A2
A1
A-ELECTRODES (6)
m,1
m,2
m,n
2,1
2,2
2,n
1,1
1,2
1,n
CONTROLLER
582
ADDRESS SELECTOR
554
564
Y-DRIVER
53
SCAN SELECTOR
563
3-LINE-JUMP SCAN SEQUENCER
562
1-LINE-JUMP SCAN SEQUENCER
SEQUENTIAL SCAN SEQUENCER
561
REFERENCE SETTER
583
DETECTOR
581
SEQUENTIAL ADDRESS GENERATOR
1-LINE-JUMP ADDRESS GENERATOR
3-LINE-JUMP ADDRESS GENERATOR
551
552
553
COUNTER
54
CLR
SCLOCK

Fig.18

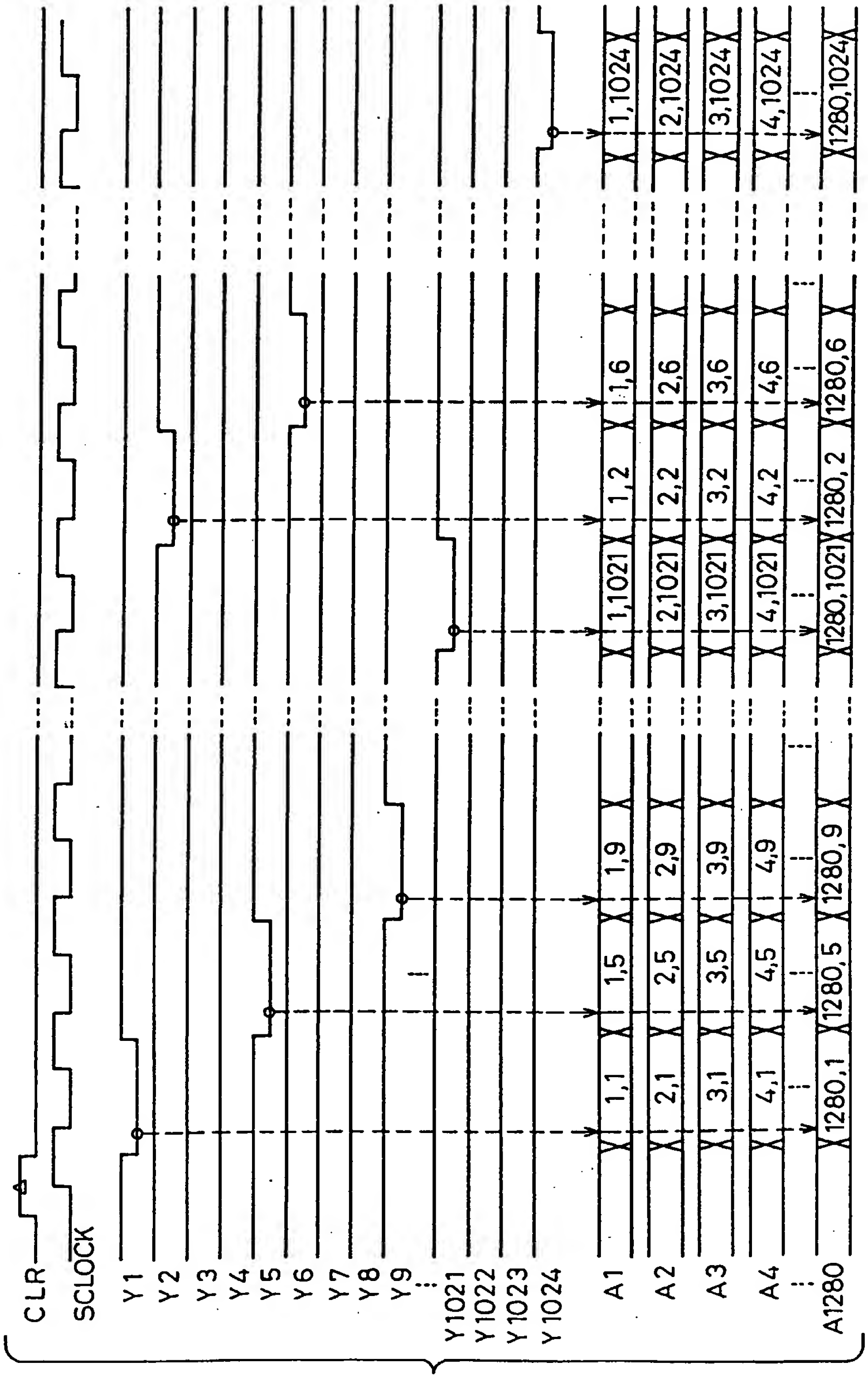

CLR
SCLOCK
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Y1021
Y1022
Y1023
Y1024
A1
A2
A3
A4
A1280
1,1
1,5
1,9
1,1021
1,2
1,6
1,1024
2,1
2,5
2,9
2,1021
2,2
2,6
2,1024
3,1
3,5
3,9
3,1021
3,2
3,6
3,1024
4,1
4,5
4,9
4,1021
4,2
4,6
4,1024
1280,1
1280,5
1280,9
1280,1021
1280,2
1280,6
1280,1024

Fig.19

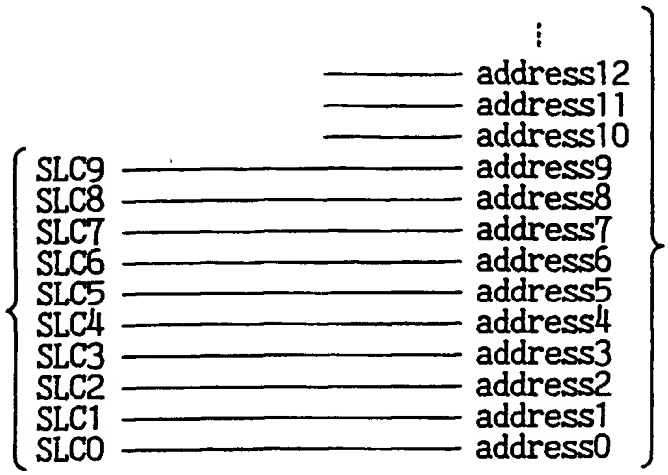

address12
address11
address10
SLC9
address9
SLC8
address8
SLC7
address7
SLC6
address6
SLC5
address5
SLC4
address4
SLC3
address3
SLC2
address2
SLC1
address1
SLC0
address0

Fig.20

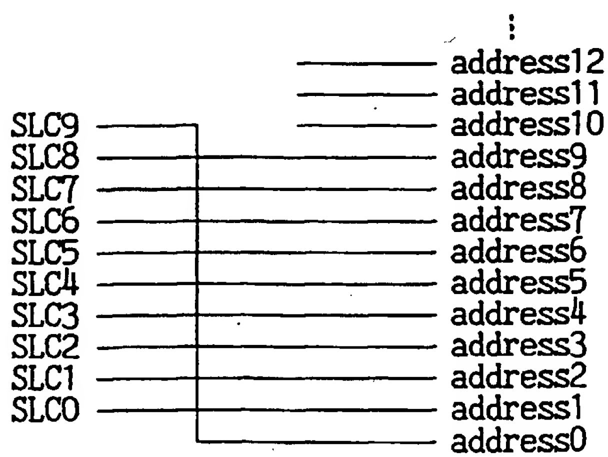

address12
address11
SLC9
address10
SLC8
address9
SLC7
address8
SLC6
address7
SLC5
address6
SLC4
address5
SLC3
address4
SLC2
address3
SLC1
address2
SLC0
address1
address0

Fig. 21

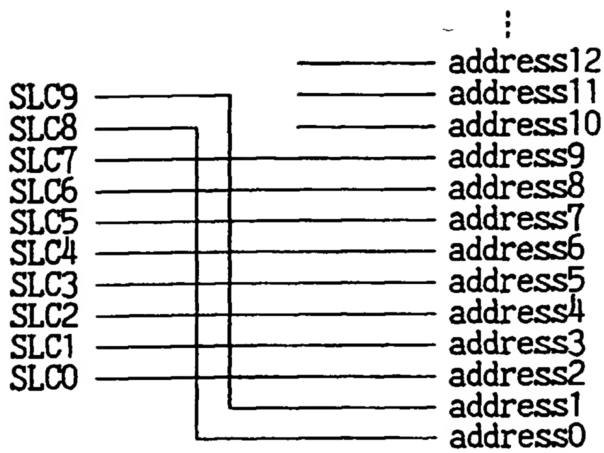
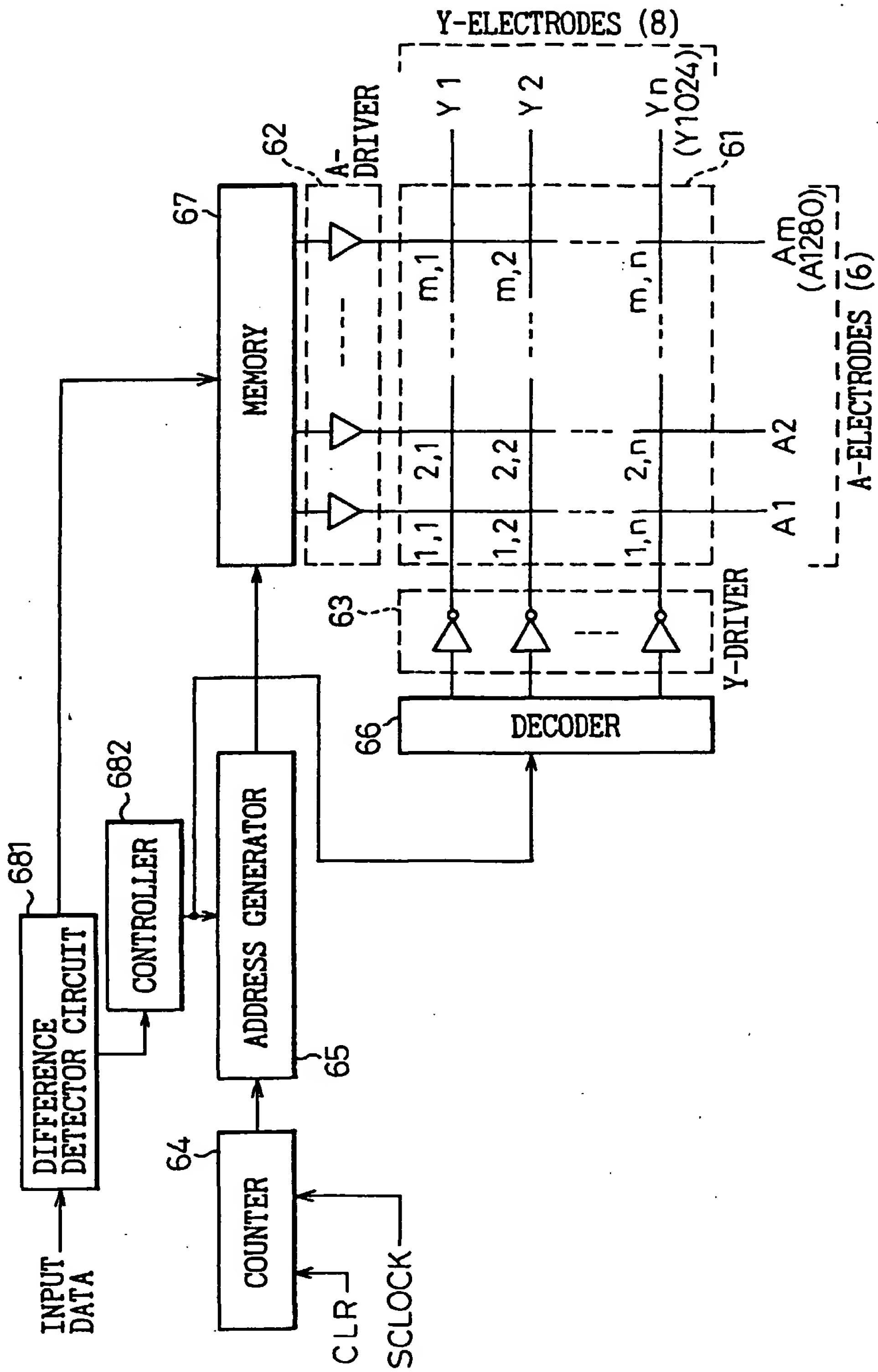
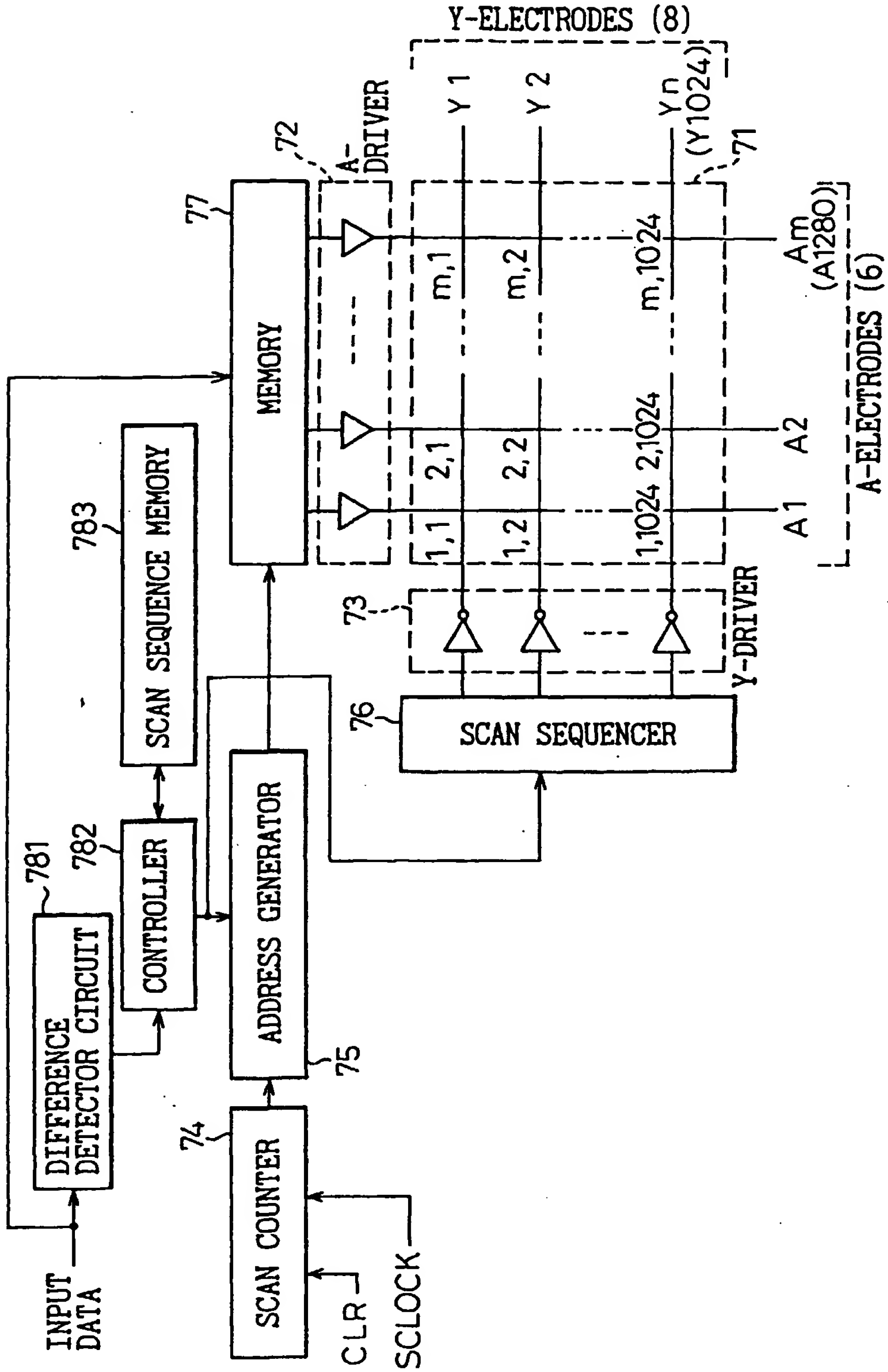

SLC9
SLC8
SLC7
SLC6
SLC5
SLC4
SLC3
SLC2
SLC1
SLC0
address12
address11
address10
address9
address8
address7
address6
address5
address4
address3
address2
address1
address0

Fig. 22



INPUT DATA
DIFFERENCE DETECTOR CIRCUIT
681
CONTROLLER
682
COUNTER
64
CLR
SCLOCK
ADDRESS GENERATOR
65
MEMORY
67
62
A-DRIVER
DECODER
66
Y-DRIVER
63
Y-ELECTRODES (8)
Y1
Y2
Yn
(Y1024)
61
A1
A2
Am
(A1280)
A-ELECTRODES (6)
1,1
2,1
m,1
1,2
2,2
m,2
1,n
2,n
m,n

Fig.23


Y-ELECTRODES (8)
Y 1
Y 2
Yn (Y1024)
71
72
A-DRIVER
77
MEMORY
Am (A1280)
A2
A1
A-ELECTRODES (6)
m,1
m,2
m,1024
2,1
2,2
2,1024
1,1
1,2
1,1024
73
Y-DRIVER
783
SCAN SEQUENCE MEMORY
76
SCAN SEQUENCER
781
782
DIFFERENCE DETECTOR CIRCUIT
CONTROLLER
ADDRESS GENERATOR
75
74
SCAN COUNTER
INPUT DATA
CLR
SCLOCK

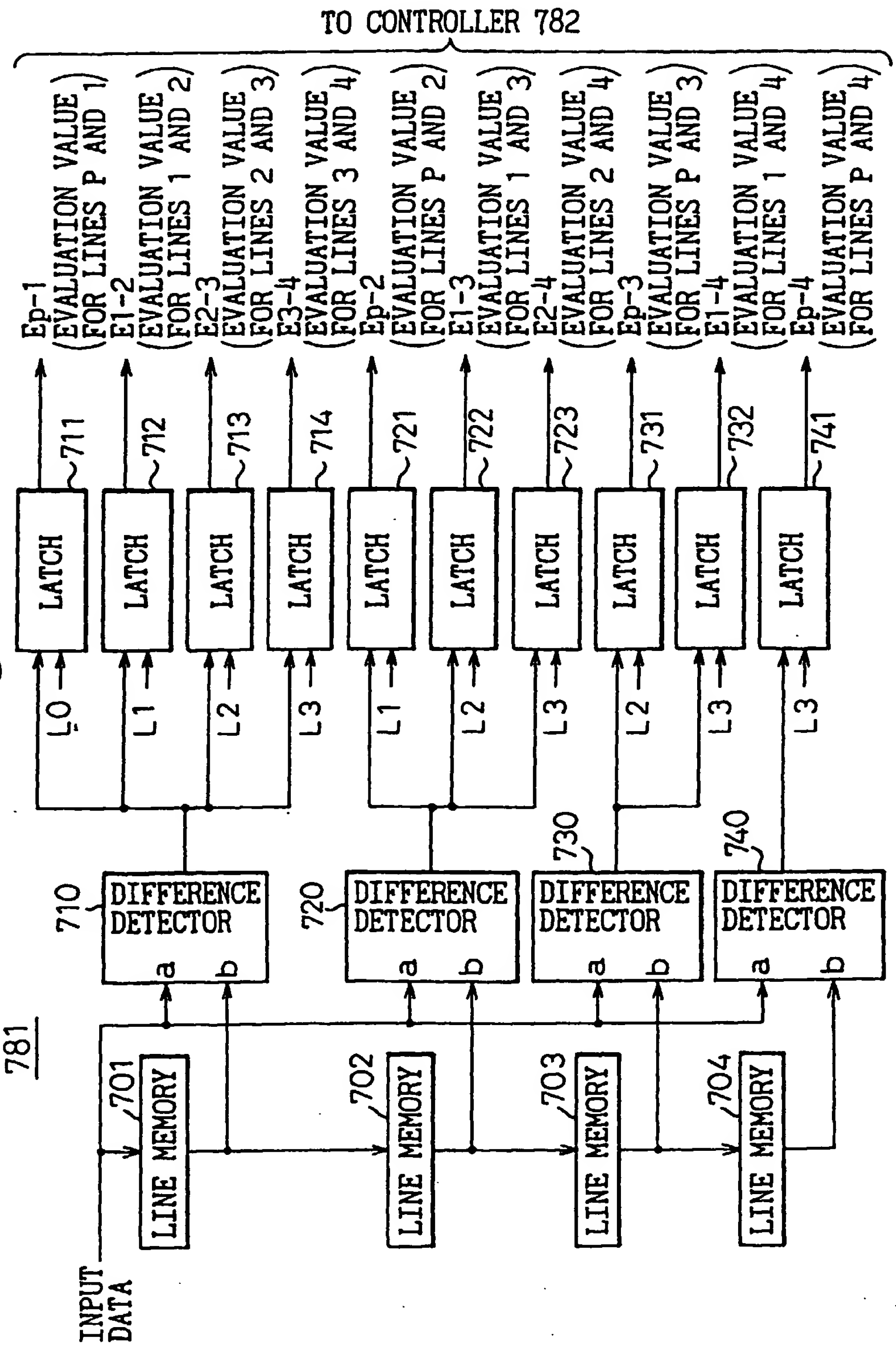

TO CONTROLLER 782
Ep-1 (EVALUATION VALUE FOR LINES P AND 1)
E1-2 (EVALUATION VALUE FOR LINES 1 AND 2)
E2-3 (EVALUATION VALUE FOR LINES 2 AND 3)
E3-4 (EVALUATION VALUE FOR LINES 3 AND 4)
Ep-2 (EVALUATION VALUE FOR LINES P AND 2)
E1-3 (EVALUATION VALUE FOR LINES 1 AND 3)
E2-4 (EVALUATION VALUE FOR LINES 2 AND 4)
Ep-3 (EVALUATION VALUE FOR LINES P AND 3)
E1-4 (EVALUATION VALUE FOR LINES 1 AND 4)
Ep-4 (EVALUATION VALUE FOR LINES P AND 4)
LATCH
711
712
713
714
721
722
723
731
732
741
L0
L1
L2
L3
DIFFERENCE DETECTOR
710
720
730
740
a
b
781
INPUT DATA
LINE MEMORY
701
702
703
704

Fig. 24

Fig.25

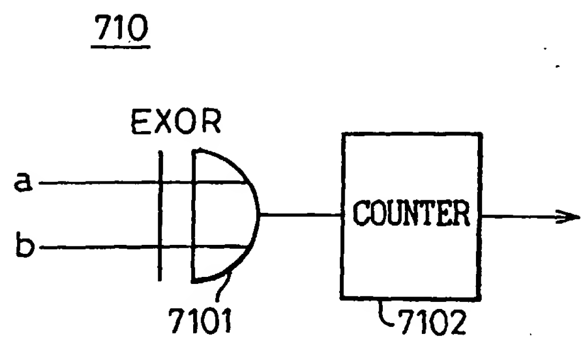

710
EXOR
a
b
COUNTER
7101
7102

Fig.26

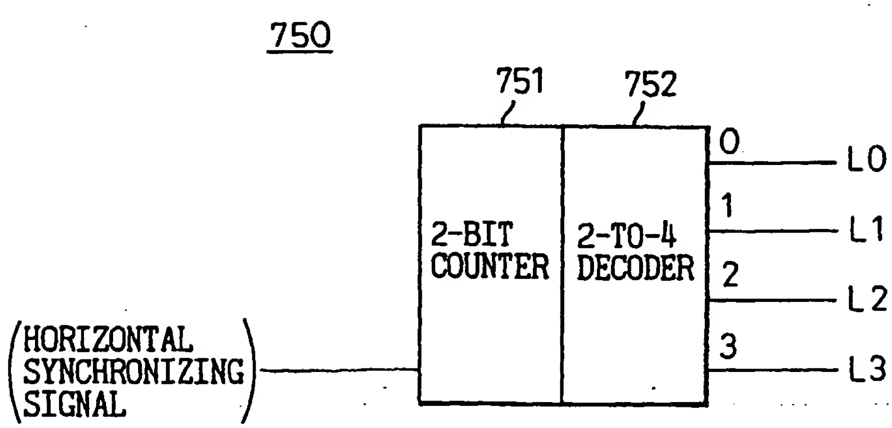

750
751
752
2-BIT COUNTER
2-TO-4 DECODER
0
1
2
3
L0
L1
L2
L3
(HORIZONTAL SYNCHRONIZING SIGNAL)

Fig.27

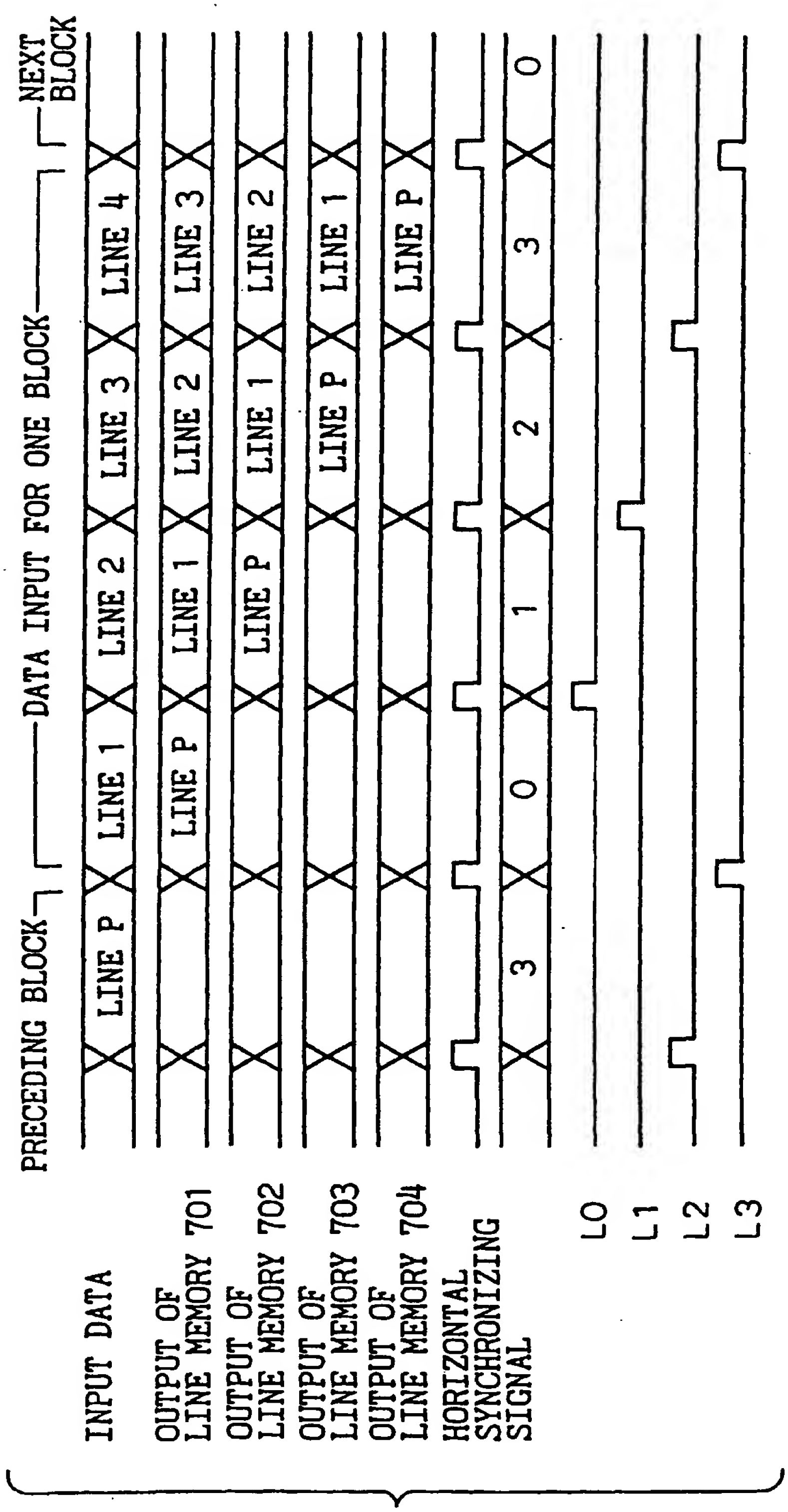

PRECEDING BLOCK
DATA INPUT FOR ONE BLOCK
NEXT BLOCK
INPUT DATA
OUTPUT OF LINE MEMORY 701
OUTPUT OF LINE MEMORY 702
OUTPUT OF LINE MEMORY 703
OUTPUT OF LINE MEMORY 704
HORIZONTAL SYNCHRONIZING SIGNAL
L0
L1
L2
L3
LINE P
LINE 1
LINE 2
LINE 3
LINE 4
LINE P
LINE 1
LINE 2
LINE 3
LINE P
LINE 1
LINE 2
LINE P
LINE 1
LINE P
3
0
1
2
3
0

Fig.28

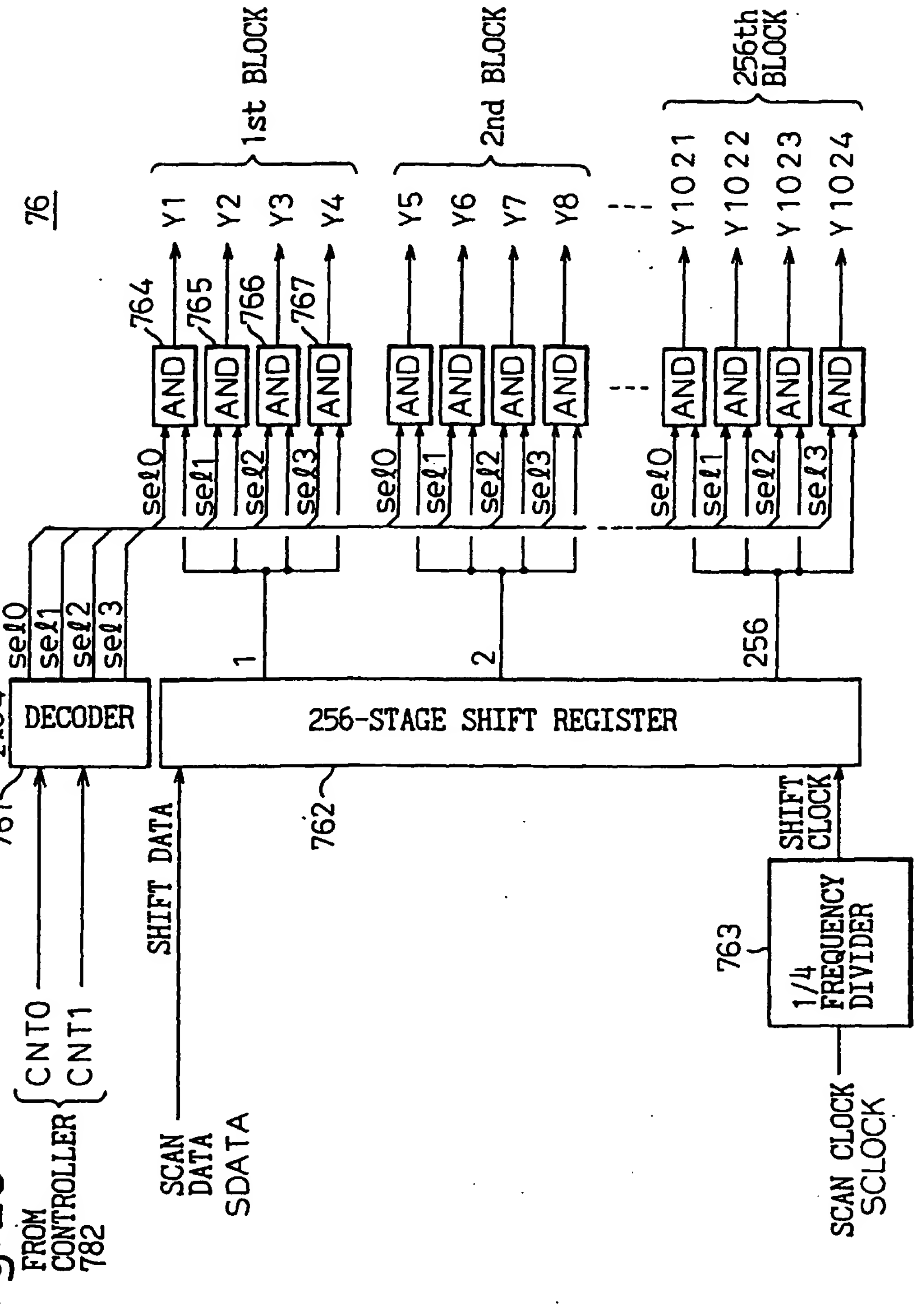
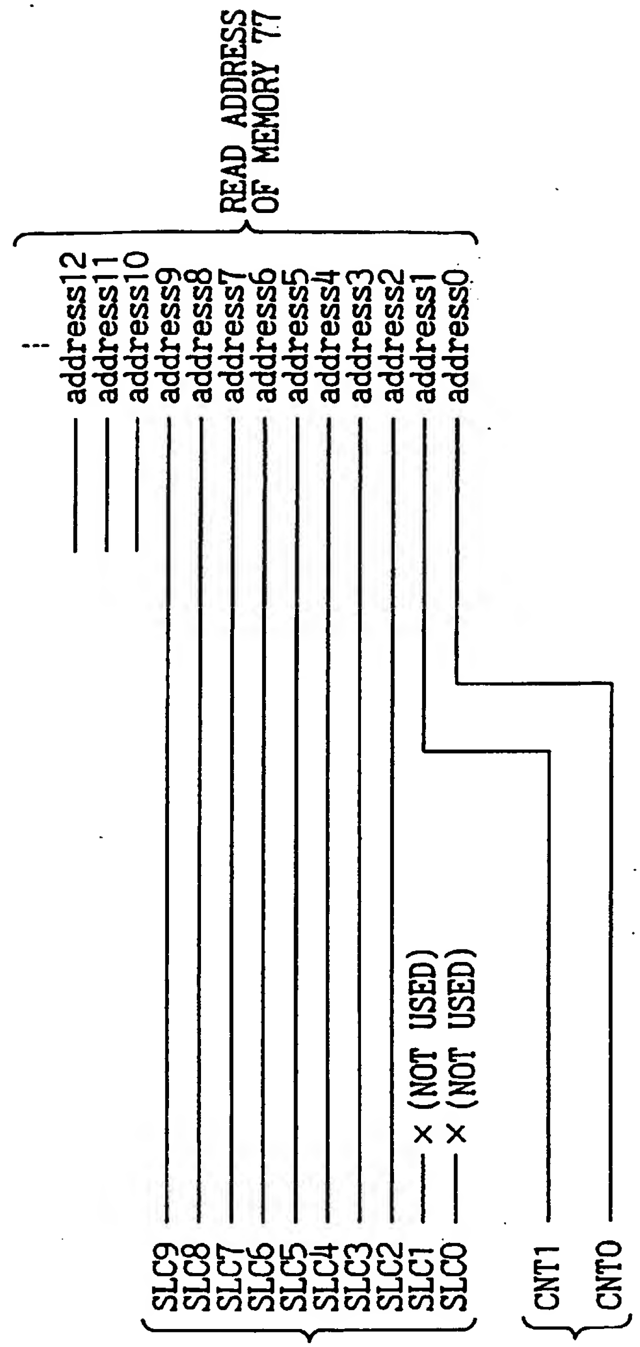

76
1st BLOCK
2nd BLOCK
256th BLOCK
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y1021
Y1022
Y1023
Y1024
764
765
766
767
AND
sel0
sel1
sel2
sel3
2to4
DECODER
761
256-STAGE SHIFT REGISTER
1
2
256
762
SHIFT DATA
SHIFT CLOCK
763
1/4 FREQUENCY DIVIDER
FROM CONTROLLER 782
CNT0
CNT1
SCAN DATA SDATA
SCAN CLOCK SCLOCK

Fig.29


READ ADDRESS OF MEMORY 77
address12
address11
address10
address9
address8
address7
address6
address5
address4
address3
address2
address1
address0
SLC9
SLC8
SLC7
SLC6
SLC5
SLC4
SLC3
SLC2
SLC1
SLC0
× (NOT USED)
× (NOT USED)
CNT1
CNT0